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Dear Member

IEC COMMITTEE DRAFT (CD)

REPLY TO CSC@BSIGROUP.COM BEFORE 1 MARCH 2017

Please find attached:

91/1421/CD - IEC 60194-2 ED1: Printed boards design, manufacture and assembly - Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies

IEC National Committees have been invited to comment on the above document. As a member of the responsible BSI committee you are asked to give your comments on the document. Please send any comments that you wish to be considered for submission as UK comments to IEC by the above date.

When submitting comments please ensure that they are entered into the [IEC comments template](#). If you have any queries in how to use the template then please do not hesitate to contact the Committee Service Centre.

It should be noted that this is often the final stage for the submission of major technical comment on the standard, as the national comments submitted to IEC determine whether this standard can progress to the next stage, i.e. circulation as a draft international standard (CDV).

Please also bear in mind that acceptance of a draft IEC standard means agreement in principle to it being the basis of a new British Standard, as it is BSI policy to implement all IEC projects as BS IEC standards unless any of the following situations apply:

- UK voted negatively at the FDIS stage.
- There is a current BS which covers the scope of the international standard and the BS continues to be the preferred document at the national level.
- There is an implemented EN standard covering the scope of the international publication.
- The International standard is subsequently agreed for UAP procedure in CLC and publication of the EN is expected within 12 months of the availability of the IEC publication.

If we do not hear from you by the above date we will submit 'no comment' to the IEC.

Yours sincerely,

Committee Service Centre



PROJECT NUMBER: IEC 60194-2 ED1	
DATE OF CIRCULATION: 2017-01-06	CLOSING DATE FOR COMMENTS: 2017-03-31
SUPERSEDES DOCUMENTS: 91/1420/RR	

IEC TC 91 : ELECTRONICS ASSEMBLY TECHNOLOGY	
SECRETARIAT: Japan	SECRETARY: Mr Masahide Okamoto
OF INTEREST TO THE FOLLOWING COMMITTEES: TC 40,TC 47,SC 47A,SC 47D	PROPOSED HORIZONTAL STANDARD: <input type="checkbox"/> Other TC/SCs are requested to indicate their interest, if any, in this CD to the secretary.
FUNCTIONS CONCERNED: <input type="checkbox"/> EMC <input type="checkbox"/> ENVIRONMENT <input type="checkbox"/> QUALITY ASSURANCE <input type="checkbox"/> SAFETY	

This document is still under study and subject to change. It should not be used for reference purposes.

Recipients of this document are invited to submit, with their comments, notification of any relevant patent rights of which they are aware and to provide supporting documentation.

TITLE: Printed boards design, manufacture and assembly - Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies

NOTE FROM TC/SC OFFICERS: This document is the revision of IEC 60194:2015 Printed board design, manufacture and assembly - Terms and definitions, which defines the terminology used in the field of printed circuit boards and printed circuit board assembly products. It is agreed to split the new revision into two separate documents. This draft is the second part of the revision. It is composed of terms and definitions related with TC91 technology as well as other technologies. In addition, the title was changed to 'Printed Boards design, manufacture and assembly - Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies'. It was approved at TC91 Plenary meeting in Frankfurt on 2016-10-14.
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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**PRINTED BOARDS DESIGN, MANUFACTURE AND ASSEMBLY -
VOCABULARY**

**PART 2: COMMON USAGE IN ELECTRONIC TECHNOLOGIES AS WELL AS
PRINTED BOARD AND ELECTRONIC ASSEMBLY TECHNOLOGIES**

FOREWORD

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International Standard IEC 60194 has been prepared by IEC technical committee 91: Electronics assembly technology.

The committee decided to split the seventh edition into two separate documents. This draft is the second part of the seventh edition. It is composed of terms and definitions related with TC91 technology as well as other technologies

This document together with Part 1 of IEC 60194 will replace IEC 60194 Ed.6.0 published in 2015-04 and constitutes technical and editorial revisions. The main changes from the previous edition are as follows:

- Exclusion of 32 general terms better served by other TCs
- Exclusion of 47 terms no longer used by electronic assembly industry
- Inclusion of 13 new terms related with device embedded substrate technology
- Removal of identification codes for terms as well as Annex

98 The text of this International Standard is based on the following documents:

FDIS	Report on voting
XX/XX/FDIS	XX/XX/RVD

99

100 Full information on the voting for the approval of this International Standard can be found in
101 the report on voting indicated in the above table.

102 This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

103 The committee has decided that the contents of this document will remain unchanged until the
104 stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to
105 the specific document. At this date, the document will be

- 106 • reconfirmed,
- 107 • withdrawn,
- 108 • replaced by a revised edition, or
- 109 • amended.

110

111 The National Committees are requested to note that for this document the stability date
112 is 2023.

113 THIS TEXT IS INCLUDED FOR THE INFORMATION OF THE NATIONAL COMMITTEES AND WILL BE
114 DELETED AT THE PUBLICATION STAGE.

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131 **PRINTED BOARDS DESIGN, MANUFACTURE AND ASSEMBLY -**
132 **VOCABULARY**
133 **PART 2: COMMON USAGE IN ELECTRONIC TECHNOLOGIES AS WELL AS**
134 **PRINTED BOARD AND ELECTRONIC ASSEMBLY TECHNOLOGIES.**
135

136 **1 Scope**

137 This part of IEC 60194 covers terms and definitions related with TC91 technology as well as
138 other technologies.

139 **2 Normative references**

140 The following documents are referred to in the text in such a way that some or all of their
141 content constitutes requirements of this document. For dated references, only the edition
142 cited applies. For undated references, the latest edition of the referenced document (including
143 any amendments) applies.

144 IEC 60050, *International Electrotechnical Vocabulary*

145 **3 Terms and definitions**

146 For the purposes of electronics assembly technology the following terms and definitions apply.

147 **4 A**

148 **abrasive trimming**

149 adjusting the value of a film component by notching it with a finely adjusted stream of an
150 abrasive material against the resistor surface

151 **accelerated ageing**

152 **accelerated life test**

153 test in which the parameters such as voltage and temperature are increased above normal
154 operating values to obtain observable or measurable deterioration in a relatively short period
155 of time

156 **accelerated test**

157 test to check the life expectancy of an electronic component or electronic assembly in a short
158 period of time by applying physically severe condition(s) to the unit under test

159 **acceleration factor**

160 **AF**

161 ratio of stress in reliability testing to the normal operating condition

162 **acceptance inspection**

163 <criteria> inspection that determines conformance of a product to design specifications as
164 the basis for acceptance

165 **acceptance quality level**

166 **AQL**

167 number of defects (in %) within a population (lot) at which the lot has the chance to be
168 accepted with an acceptance probability of about 90 % when testing a sample

169 **acceptance tests**

170 tests deemed necessary to determine the acceptability of a product as agreed to by both
171 purchaser and vendor

172 **accuracy**

173 degree to which the result of a measurement or calculation agrees with the true value

174 **active device**

175 electronic component whose basic character changes while operating on an applied signal

176 Note 1 to entry: This includes diodes, transistors, thyristors, and integrated circuits that are used for the
177 rectification, amplification, switching, etc., of analog or digital circuits in either monolithic or hybrid form.

178 **add-on component**

179 discrete or integrated packaged or chip components that are attached to a film circuit in order
180 to complete the circuit's function

181 **adhesive**

182 non-metallic materials that can join solids by surface bonding and internal strength (adhesion
183 and cohesion)

184 Note 1 to entry: In surface mounting, an epoxy adhesive is used to adhere SMDs to the substrate.

185 (SOURCE:IEC 60050-212:2010, 212-15-44)

186 **all metal package**

187 hybrid circuit package made solely of metal, without glass or ceramic

188 **allowable temperature**

189 temperature range in which an electronic circuit or component can perform its intended
190 functions

191 **alphanumeric**

192 pertaining to data that contain the letters of an alphabet, the decimal digits, and may contain
193 control characters, special characters and the space character

194 **alpha particle**

195 He⁴ nucleus generated from a nuclear decay that is capable of generating hole-electron pairs
196 in microelectronic devices and switching cells causing soft errors in some devices

197 **alternating current**

198 **AC**

199 electric current that is a periodic function of time with a zero direct component or, by
200 extension, a negligible direct component

201 Note 1 to entry: For the qualifier AC, see IEC 60050-151.

202 (SOURCE:IEC 60050-131:2002, 131-11-24)

203 **ambient**

204 surrounding environment coming into contact with the system or component in question

205 **amplitude**

206 <voltage> maximum value of a voltage of an alternating voltage within one period

207 **analog circuit**

208 electrical circuit that provides a continuous relationship between its input and output

209 **anisotropy**

210 condition for a substance having differing values for properties, such as permittivity,
211 depending on the direction within the material

212 **anode**

213 **BGA**

214 electrode capable of emitting positive charge carriers to and/or receiving negative charge
215 carriers from the medium of lower conductivity

216 Note 1 to entry: The direction of electric current is from the external circuit, through the anode, to the medium of
217 lower conductivity.

218 Note 2 to entry: In some cases (e.g. electrochemical cells), the term "anode" is applied to one or another
219 electrode, depending on the electric operating condition of the device. In other cases (e.g. electronic tubes and
220 semiconductor devices), the term "anode" is assigned to a specific electrode.

221

222 (SOURCE:IEC 60050-151:2001, 151-13-02)

- 223 **application specific integrated circuit**
224 **ASIC**
225 integrated circuit designed for specific applications
226 (SOURCE:IEC 60050-521:2002, 521-11-18)
- 227 **area array package**
228 package that has terminations arranged in a grid on the bottom of the package and contained
229 within the package outline
- 230 **assembly**
231 **assembled board**
232 number of parts, subassemblies or combinations thereof joined together
- 233 Note 1 to entry: This term can be used in conjunction with other terms listed herein, for example, "printed board
234 assembly".
- 235 **attenuation**
236 the decrease of the energy of an electromagnetic wave during its propagation, represented
237 quantitatively by the ratio of the power flux densities at two specified points
- 238 Note 1 to entry: Attenuation is generally expressed in decibels.
239 (SOURCE:IEC 60050-705:1995, 705-02-05)
- 240 **5 B**
- 241 **backfill**
242 filling a hybrid circuit package with a dry inert gas prior to hermetic sealing
- 243 **backplane**
244 **backpanel**
245 an interconnection device used to provide point-to-point electrical interconnections
- 246 Note 1 to entry: It is usually a printed board that has discrete wiring terminals on one side and connector
247 receptacles on the other side.
248 Note 2 to entry: See also "mother board".
- 249 **backward crosstalk**
250 **near-end crosstalk**
251 noise induced into an adjacent line, as seen at that end of the adjacent line which is closest to
252 the signal source, when this line has been placed near an active line
- 253 Note 1 to entry: See also "forward crosstalk".
- 254 **balanced transmission line**
255 transmission line that has distributed inductance, capacitance, resistance, and conductance
256 elements that are equally distributed between its conductors
- 257 **ball**
258 raised metal (or other conductive material) feature on a package substrate used to facilitate
259 bonding to the next level of interconnect
- 260 **ball grid array**
261 **BGA**
262 surface-mount package wherein the bumps for terminations are formed in a grid on the bottom
263 of a package
- 264 SEE: Figure 1.

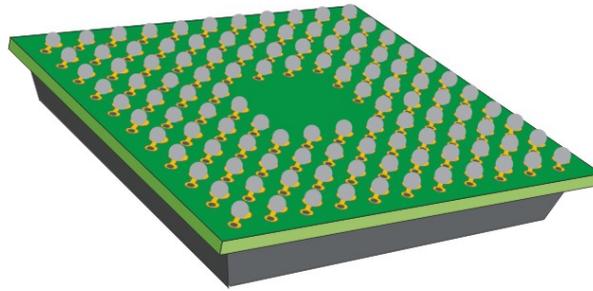


Figure 1 – Ball grid array (BGA)

265

266

267 **barcode**

268 linear arrangement of bars and spaces in a predetermined pattern

269 **barcode marking**

270 identification code consisting of a pattern of vertical bars whose width and spacing identifies
271 the item marked

272 **barcode symbol**

273 print of photographically reproduced barcode composed of parallel bars and spaces of various
274 widths

275 Note 1 to entry: A barcode symbol contains a leading quiet zone, a start character, data characters, a stop
276 character, and a trailing quiet zone; in some cases, a check character is included.

277 **bare die**

278 unpackaged discrete semiconductor or integrated circuit with pads on the upper surface
279 suitable for interconnection to the substrate or package

280 **base film**

281 <relating to flexible circuits> film that is the base material for the flexible printed wiring board
282 and on the surface of which the conductive pattern can be formed

283 Note 1 to entry: When the heat resistance is required, polyimide film is mostly used, and polyester film is usually
284 used when the heat resistance is not required.

285 **base material**

286 **substrate**

287 the insulating material upon which a conductive pattern may be formed

288 Note 1 to entry: The base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.

289 **base material thickness**

290 thickness of the base material excluding conductive foil or material deposited on the surfaces

291 **base plane**

292 plane that includes the lowest point of the mounting surface of the package, except for
293 packages using stand-offs

294 **basic specification**

295 **BS**

296 document that describes the common elements for a set, family or group of products,
297 materials, or services

298 **bending resistance**

299 ability of a material to withstand repeated bending to specified parameters without producing
300 cracks and breaks in excess of the specification allowance

301 **bias**

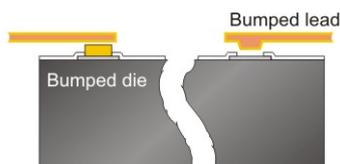
302 <fabric> filling yarn that is off-square with the warp ends of a fabric

303 **bipolar device**

304 device in which both majority and minority carriers are present

305 Note 1 to entry: Bi-polar and Metal-Oxide Semi-conductor (MOS) are the two most common device types.

- 306 **bond**
307 interconnection that performs a permanent electrical and/or mechanical function
- 308 **bond pads**
309 metallised areas on the die that are used for temporary or permanent electrical connection
310 (bonding)
- 311 **bond strength**
312 **pull strength**
313 force perpendicular to a board's surface required to separate two adjacent layers of the board
- 314 Note 1 to entry: Bond strength is expressed as force per unit area.
- 315 **bonding pad**
316 <IC> area of metallization on an integrated circuit die that permits connection of fine wires or
317 a circuit element to the die
- 318 **bonding wire**
319 gold or aluminum wire used for making electrical connections between lands, lead frames,
320 and terminals
- 321 **bow**
322 **warp**
323 <fabric> filling yarn that lies in an arc across the width of a fabric
- 324 **break-down voltage**
325 voltage at which the insulation between two conductors ruptures
- 326 **bridging**
327 <electrical>unintentional formation of a conductive path between conductors
- 328 Note 1 to entry: See also “solder bridging”.
- 329 **bulk packaging**
330 method for packaging loose parts, into a bag or case
- 331 **bumped die**
332 semiconductor die with raised metal features that facilitate inner-lead bonding. (See Figure 2).



333
334 **Figure 2 – Bumped Die**

- 335 **burn-in**
336 process of electrically stressing a device at an elevated temperature, for a sufficient amount
337 of time to cause the failure of marginal devices (infant mortality)
- 338 **burn-in**
339 <dynamic>burn-in at high temperatures that simulates the effects of actual or simulated
340 operating conditions
- 341 **burn-in**
342 <static>burn-in at high temperatures with unvarying voltage, either forward or reverse bias
- 343 **6 C**
- 344 **capacitance**
345 measure of the ability of two adjacent conductors separated by an insulator to hold a charge
346 when a voltage is impressed between them
- 347 (SOURCE:IEC 60050-131:2008, 131-12-13)

348 **capacitive coupling**
 349 electrical interaction between two conductors that is caused by the capacitance between them

350 **ceramic dual-in-line package**
 351 **CERDIP**
 352 dual in-line-package that has a package body of ceramic material and is hermetically sealed
 353 by a glass

354 Note 1 to entry: See also “dual-in-line package”.

355 **ceramic pin grid array**
 356 **ceramic PGA**
 357 pin grid array package (PGA) made of a ceramic material, hermetically sealed by metal, with
 358 leads formed on a grid extending from the bottom of the package

359 **ceramic quad flat package**
 360 **CQFP**
 361 quad flat package (QFP) made of a ceramic material, hermetically sealed by metal, with leads
 362 extending from all four sides

363 **certification**
 364 verification that specified training or testing has been performed and that required proficiency
 365 or parameter values have been attained

366 **characteristic impedance**
 367 a quantity defined for a mode of propagation at a given frequency in a specific uniform
 368 transmission line or uniform waveguide by one of the three following relations:

369 $Z_1 = S / |I|^2$
 370 $Z_2 = |U|^2 / S$
 371 $Z_3 = U / I$

372 where Z is the complex characteristic impedance, S the complex power and U and I are the
 373 values, usually complex, respectively of a voltage and a current conventionally defined for
 374 each type of mode by analogy with transmission line equations

375 Examples:

376 1. — For a parallel-wire transmission line, U and I can be uniquely defined and the three equations are consistent.
 377 If the transmission line is lossless, the characteristic impedance is real.

378 2. — For a waveguide, the conventional definitions for U and I depend on the type of mode and generally lead to
 379 three different values of the characteristic impedance.

380 3. — For a circular waveguide in the dominant mode TE_{11} , U = r.m.s. voltage along the diameter where the
 381 magnitude of the electric field strength vector is a maximum, I = the r.m.s. longitudinal current.

382 4. — For a rectangular waveguide in the dominant mode TE_{10} , U = the r.m.s. voltage between midpoints of the two
 383 conductor faces normal to the electric field strength vector, I = the r.m.s. longitudinal current following on one
 384 surface normal to the electric field strength vector.

385 (SOURCE:IEC 60050-726:1982, 726-07-01)

386 **chemical vapour deposition**
 387 process in which vapours and gases react chemically to produce deposits at the surface of a substrate

388 (SOURCE:IEC 60050-841:2004, 841-22-07)

389 **chip**
 390 see “die”

391 Note 1 to entry: Common parlance for die.

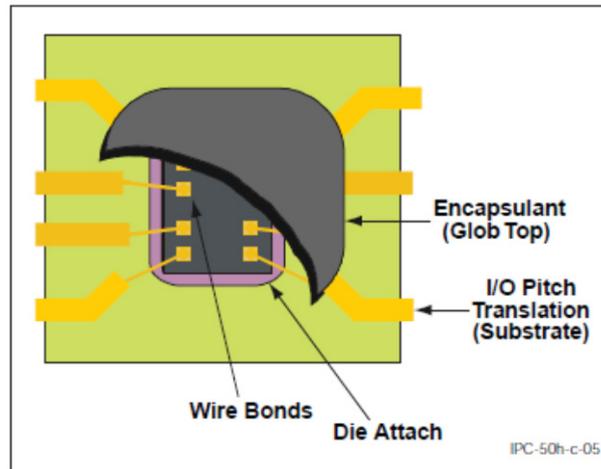
392 **chip carrier**
 393 low-profile, usually square, surface-mount component semiconductor package whose die
 394 cavity or die mounting area is a large fraction of the package size and whose external
 395 connections are usually on all four sides of the package

396 Note 1 to entry: It may be leaded or leadless.

397 **chip-on-board**398 **COB**

399 printed board assembly technology that places unpackaged semiconductor dices and
 400 interconnects them by wire bonding or similar attachment techniques

401 SEE: Figure 3.



402

403 **Figure 3 – Chip on board (COB)**

404 Note 1 to entry: The silicon area density is usually smaller than the density of the printed board.

405 Note 2 to entry: A mounting and attachment technique where the die is mounted onto a substrate, often a printed-
 406 circuit board.

407 **chip-on-flex**408 **COF**

409 semiconductor chip mounted directly onto a flexible printed board

410 **chip-on-glass**411 **COG**

412 assembly technology that uses an unpackaged semiconductor die mounted directly on a glass
 413 substrate such as a glass plate for liquid crystal display (LCD)

414 **chip scale package**415 **CSP**

416 generic term for packaging technologies that result in a packaged part that is only marginally
 417 larger than the internal die

418 **circuit**

419 number of electrical elements and devices that have been interconnected to perform a desired
 420 electrical function

421 **CMOS**

422 complementary metal oxide semiconductor

423 fabrication technology that results in the creation of both NMOS and PMOS FET devices

424 **coaxial cable**

425 cable in the form of a central wire surrounded by a conductor tubing or sheathing that serves
 426 as a shield and return

427 **compensation circuit**

428 electrical circuit that alters the functioning of another circuit to which it is applied to achieve a
 429 desired performance

430 **component**

431 individual part or combination of parts that, when together, perform (a) design function(s)

432 Note 1 to entry: (See also "discrete component").

433 **component mounting site**

434 location on a packaging and interconnecting structure (P&I) that consists of a land pattern and
 435 conductor fan-out to additional lands for testing or vias that are associated with the mounting
 436 of a single component

437 **compression seal**

438 tight joint made between a component package and its leads that is formed as heated metal
 439 cools and shrinks around a glass insulator

440 **computer-aided design**441 **CAD**

442 interactive use of computer systems, programs, and procedures in the design process
 443 wherein, the decision-making activity rests with the human operator and a computer provides
 444 the data manipulation function

445 **conditioning**

446 subjection of a specimen for a specified duration to specific climatic conditions (usually a
 447 specified temperature and a specified relative humidity) or to an atmosphere of specified
 448 relative humidity or to complete immersion in water or other liquid

449 (SOURCE:IEC 60050-212:2010, 212-12-01)

450 **conductance**

451 for a resistive two-terminal element or two-terminal circuit with terminals A and B, quotient of
 452 the electric current i in the element or circuit by the voltage u_{AB} (131-11-56) between the
 453 terminals

$$G = \frac{i}{u_{AB}}$$

454

455 where the electric current is taken positive if its direction is from A to B and negative if its
 456 direction is from B to A

457 Note 1 to entry: The conductance of an element or circuit is the inverse of its resistance.

458 Note 2 to entry: The term "conductance" is also a short term for "conductance to alternating current" (131-12-53).

459 Note 3 to entry: The coherent SI unit of conductance is siemens, S.

460 (SOURCE:IEC 60050-131:2013, 131-12-06)

461 **conductive ink**

462 liquid medium with a suspended powder of an electrically conductive material

463 **conductive medium**

464 material with a suspended powder of an electrically conductive material

465 Note 1 to entry: See also conductive paints, inks, pastes.

466 **conductive pattern**

467 conductor pattern

468 configuration formed by the electrically conductive material of a printed board

469 (SOURCE:IEC 60050-514:1900, 541-01-04)

470 **conductivity**

471 <electrical>ability of a substance or material to conduct electricity

472 **conductivity**

473 <thermal>ability of a substance or material to conduct heat

474 **conductor**475 **conductor line**476 **conductor path**477 **conductor track**478 **line**

- 479 **electrical path**
480 **trace**
481 **track**
482 single conductive path in a conductive pattern
483 (SOURCE:IEC 60050-541:1990, 541-01-20)
- 484 **constraining core**
485 supporting plane that is internal to a packaging and interconnecting structure
- 486 **controlled collapse soldering**
487 **controlled collapse <component connection>**
488 technique for soldering a component (i.e., flip chip, chip scale package, BGA) to a substrate,
489 where the component connection surface tension forces of the liquid solder supports the
490 weight of the component and controls the height of the joint
- 491 **coplanar leads**
492 flat beam leads of a component package that have been formed so that they can
493 simultaneously contact one plane of a base material
- 494 **corona**
495 electrical discharge brought on by the ionization of a liquid surrounding a conductor, which
496 occurs when the potential gradient exceeds a certain value, but conditions are insufficient to
497 cause complete electrical breakdown or arcing
- 498 **creel**
499 device used as a yarn package rack to hold warp ends for a section beam
- 500 **critical defect**
501 any anomaly specified as being unacceptable
- 502 **crosstalk**
503 **spurious signal**
504 undesirable transfer of electrical energy between neighbouring conductors (coupling) by
505 mutual inductance and capacitance
506 Note 1 to entry: See also "backward crosstalk" and "forward crosstalk".
- 507 **cupping**
508 <BGA> condition of a ball grid array package after reflow where the corners turn up and away
509 from the printed board laminate surface
510 Note 1 to entry: This condition in the worst case causes the balls on the outside row to be in tension and the balls
511 in the centre to be in compression.
512 Note 2 to entry: Opposite of "doming (BGA)".
- 513 **current**
514 flow or movement of electrons in a conductor as the result of a voltage difference between the
515 ends of the conductive path
- 516 **current-carrying capacity**
517 maximum electrical current that can be carried continuously by a conductor, under specified
518 conditions, without causing objectable degradation of electrical and mechanical properties of
519 the product
- 520 **customer detail specification**
521 **CDS**
522 document that establishes the specific requirements, identified in a detailed specification, in
523 order to tailor these to meet the needs of a custom product, material, or service
- 524 **7 D**
- 525 **damage**
526 result of an event that degrades a product, for example, component, printed board, module,
527 etc., beyond the form, fit and function limits of the governing document

- 528 **data capture**
529 automatic collection of information from a given machine or other information source
- 530 **database**
531 comprehensive collection of information that is structured in such a way that some or all of its
532 data may be used to create queries about related items contained within it
- 533 **dead-bug**
534 orientation of a package with the terminations facing up
- 535 **decoupling**
536 absorbing of noise pulses in power supply lines, that were generated by switching logic
537 devices, so as to prevent the lines from disturbing other logic devices in the same power-
538 supply circuit
- 539 **defect**
540 nonconformance or other risk factors as identified by the manufacturer
- 541 Note 1 to entry: A process and/or material non-conformance that could result in a reduction of functional
542 capability, design life or reliability.
- 543 **degradation**
544 an undesired departure in the operational performance of any device, equipment or system
545 from its intended performance
- 546 Note 1 to entry: The term "degradation" can apply to temporary or permanent failure.
547 (SOURCE:IEC 60050-161:1990, 161-01-19)
- 548 **detail specification**
549 detailed written description of a part or a process
- 550 **dice**
551 two or more die
- 552 **dicing**
553 separating of semi-conductor wafers into individual die
- 554 **die**
555 **chip**
556 **leadless device**
557 separated part (or whole) of a wafer intended to perform a function or functions in a device
558 (SOURCE:IEC 60050-521:2002, 521-05-30)
- 559 **die bonding**
560 attachment of a die to base material
- 561 **die device**
562 bare die, with or without connection structures, or a minimally packaged die
- 563 **dielectric strength**
564 maximum voltage that a dielectric can withstand under specified conditions without a voltage
565 breakdown
- 566 Note 1 to entry: Dielectric strength is usually expressed as volts per unit dimension
- 567 **digital circuit**
568 electrical circuit that provides two (binary) or three distinct relationships (states) between its
569 input and output
- 570 **direct current**
571 **DC**
572 electric current that is time-independent or, by extension, periodic current the direct
573 component of which is of primary importance
- 574 Note 1 to entry: For the qualifier DC, see IEC 60050-151.
575 (SOURCE:IEC 60050-131:2002, 131-11-22)

576 **discrete component**
577 separate part of a printed board assembly that performs a circuit function (For example, a
578 resistor, a capacitor, a transistor, etc.)

579 **doming**
580 <BGA> condition of a ball grid array package after reflow where the corners turn down and
581 toward the printed board laminate surface

582 Note 1 to entry: This condition in the worst case causes the balls on the outside row to be compressed and the
583 balls in the centre to be in tension.

584 Note 2 to entry: Opposite of “cupping BGA”.

585 **doping**
586 addition of a specific impurity to a slice of silicon monocrystal to alter the conductivity of the
587 crystal in a specified manner in order to produce semiconductor devices from this crystal

588 **double-sided assembly**
589 packaging and interconnecting structure with components mounted on both the primary and
590 secondary sides

591 Note 1 to entry: See also “single-sided assembly”.

592 **dry pack**
593 container that maintains the moisture content of the packages of die devices within specified
594 limits

595 **dual-inline package**

596 **DIP**

597 basically rectangular component package that has a row of leads extending from each of the
598 longer sides of its body that are formed at right angles to a plane and parallel to the base of
599 its body

600 **8 E**

601 **edge-transmission attenuation**
602 loss of a logic signal's switching-edge sharpness that has been caused by the absorption of
603 the highest-frequency components by the transmission line

604 Note 1 to entry: See also “attenuation”.

605 **electrical characteristics**
606 distinguishing electrical traits or properties of a component or assembly

607 **electromagnetic compatibility**

608 **EMC**

609 ability of a device to function properly in its operating environment without causing
610 electromagnetic interference to other equipment, or itself being susceptible to external
611 interference

612 **electromagnetic interference**

613 **EMI**

614 degradation of the performance of an equipment, transmission channel or system caused by an
615 electromagnetic disturbance

616 Note 1 to entry: In French, the terms “perturbation électromagnétique” and “brouillage électromagnétique”
617 designate respectively the cause and the effect, and should not be used indiscriminately.

618 Note 2 to entry: In English, the terms “electromagnetic disturbance” and “electromagnetic interference” designate
619 respectively the cause and the effect, but they are often used indiscriminately.

620 (SOURCE:IEC 60050-161:1990, 161-01-06)

621 **electrostatic discharge**

622 **ESD**

623 a transfer of electric charge between bodies of different electrostatic potential in proximity or
624 through direct contact

625 (SOURCE:IEC 60050-161:1990, 161-01-22)

626 **9 F**627 **farad**

628 unit of electrical capacitance

629 **far-end crosstalk**

630 see “forward crosstalk”

631 **fault**

632 any condition that causes a device or circuit to fail to operate in a proper manner

633 **film conductor**634 conductor formed in place on a base material by depositing a conductive material using
635 screening, plating or evaporating techniques636 **film network**

637 electrical network composed of thin-film and/or thick-film components on a base material

638 **final inspection**639 **delivery inspection**640 evaluation of quality characteristics relating to a standard, specification, or design drawing
641 prior to shipping to the customer642 **final seal**643 manufacturing process that completes the enclosure of a microcircuit so that further internal
644 processing cannot be performed without removing a lid or otherwise disassembling the
645 package646 **fine leak**647 leak in a sealed package that is less than 0,000 01 cm³/s at one atmosphere of differential air
648 pressure649 **fine pitch QFP**

650 quad flat pack (QFP) package whose lead pitch centres at 0,635 mm or less centre

651 **flat pack**652 rectangular component package that has a row of leads extending from each of the longer
653 sides of its body that are parallel to the base of its body654 **flexible double-sided printed board**655 **double-sided flexible printed wiring board**

656 double-sided printed board using a flexible base material only

657 (SOURCE:IEC 60050-541:1990, 541-01-14)

658 **flexible material interconnect construction**659 **FMIC**660 integration of passive and active components with mechanical components (including
661 switches and connectors) on a flexible or thin base material, i.e., flexible printed board, in
662 order to produce an electronic assembly663 **flexible multilayer printed board**

664 multilayer printed board using a flexible base material only

665 Note 1 to entry: Different areas of the flexible multilayer printed board may have different numbers of layers and
666 different thicknesses and consequently different flexibility.

667 (SOURCE:IEC 60050-541:1990, 541-01-05)

668 **flexible printed board**

669 a printed board using a flexible base material only

670 Note 1 to entry: It may be partially provided with electrically non-functional stiffeners and/or coverlayers

671 (SOURCE:IEC 60050-541:1990, 541-01-12).

672 **flexible printed circuit**

673 patterned arrangement of printed circuitry and components that utilizes flexible base material
674 with or without flexible coverlayer

675 **flexible printed wiring**

676 patterned arrangement of printed wiring that utilizes flexible base material with or without
677 flexible coverlayer

678 **flexible single-sided printed board**

679 single-sided printed board using a flexible base material only

680 (SOURCE:IEC 60050-514:1990, 541-01-13)

681 **flex-rigid double-sided printed board**

682 See "rigid-flex double sided printed board"

683

684 **flex-rigid printed board**

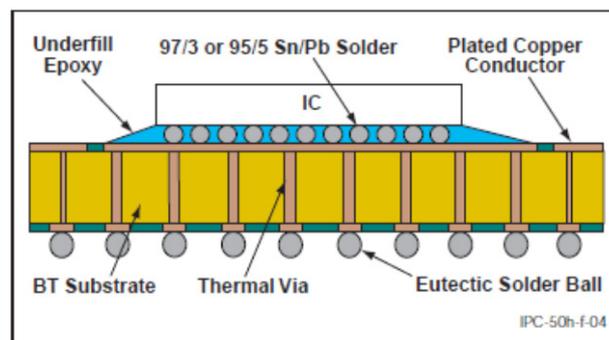
685 See "rigid-flex printed board"

686

687 **flip chip**

688 leadless monolithic circuit element structure that electrically and mechanically interconnects
689 to a printed board by conductive bumps

690 SEE: Figure 4.



691

692 **Figure 4 – Flip chip**

693 **forward crosstalk**694 **far-end crosstalk**

695 noise induced into a adjacent line, as seen at the end of the adjacent line that is the farthest
696 from the signal source, because the adjacent line has been placed next to an active line

697 Note 1 to entry: See also "backward crosstalk".

698 **frequency**

699 <electrical current> number of cycles (hertz) or completed alterations per second

700 **fully additive process**701 **fully electroless process**

702 additive process wherein the entire thickness of electrically isolated conductors is obtained by
703 the use of electroless deposition

704 Note 1 to entry: See also: "semi-additive process".

705 **10 G**706 **generic specification**707 **GS**

708 document that describes as many general requirements as possible, pertaining to a set,
709 family or group of products, materials, or service

710 **go/no-go test**

711 testing process that yields only a pass or a fail condition

712 **gross leak**

713 leak in a sealed package that is greater than 0,000 01 cm³/s at 1 atm of differential air
714 pressure

715 **ground**

716 common reference point for electrical circuit returns, shielding, or heat sinking

717 **ground plane**

718 conductor layer, or portion thereof, that serves as a common reference for electrical circuit
719 returns, shielding, or heat sinking

720 Note 1 to entry: See also "signal plane" and "voltage plane".

721 **11 H**722 **header**

723 <module> base of an electronic component package that contains leads

724 **heatsink**725 **thermal shunt**

726 mechanical device that is made of a high thermal conductivity and low specific heat material
727 that dissipates heat generated by a component or assembly

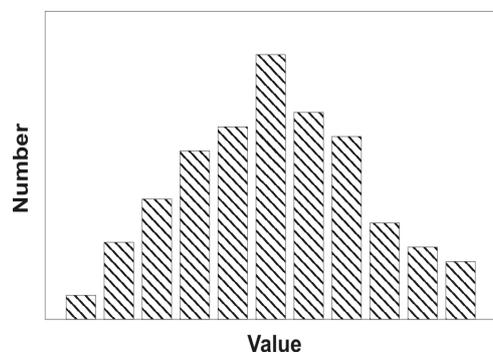
728 **hermetic**

729 <sealing> condition of sealing a component from incoming gases to a specific of inward
730 diffusion normally less than 1×10^{-6} cm³/s

731 **histogram**

732 graph that depicts values that were obtained by dividing the range of a data set into equal
733 intervals and that plots the number of data points in each interval

734 SEE: Figure 5



735
736

Figure 5 – Histogram

737 **horn**

738 cone-shaped object that transmits ultrasonic energy from a transducer to a bonding tool

739 **hybrid circuit**

740 circuit comprising insulating of base material with various combinations of interconnected film
741 conductors, film components, semiconductor die(s), passive components and bonding wire

742 Note 1 to entry: See also multi-chip module and multi-chip package.

743 **hybrid integrated circuit**

744 circuit comprising insulating base material with various combinations of interconnected film
745 conductors, film components, semiconductor dice, passive components and bonding wire that
746 perform the same function as a monolithic semiconductor integrated circuit

747 **hybrid microcircuit**

748 circuit comprising insulating base material with various combinations of interconnected film
749 conductors, film components, semiconductor dice, passive components and bonding wire

750 **12 I**751 **immersion conditions**

752 test conditions resulting when surface-mounting device package leads are immersed into a
753 solder bath to check their resistance to soldering temperatures

754 **impedance**

755 resistance set against the flow of a current in a conductor, represented by an electrical
756 network of combined ohmic resistance, capacitance and inductance, at applying an a.c.
757 source

758 Note 1 to entry: The unit for impedance is ohm, and in principle, it is equal to the square root of the sum of the
759 squares of ohmic resistance, reactance and inductance.

760 **inductance**

761 property of a conductor that allows it to store energy in a magnetic field induced by a current
762 flowing through it

763 Note 1 to entry: The unit of measure is henry (H).

764 **input vector**

765 set of logic values to be applied to the complete set of input test points at any one point in
766 time

767 **insertion loss**

768 ratio of transmitted electromagnetic power to incident power

769 Note 1 to entry: This loss of power includes losses by conversion to heat in the dielectric and in the conductors.

770 Note 2 to entry: The insertion loss is usually expressed in decibel (dB).

771 **inspection lot**

772 collection of product units that are identified and treated as a unique entity from which a
773 sample is drawn and inspected in order to determine conformance with acceptability criteria

774 **integrated circuit**

775 combination of inseparable associated circuit elements that are formed in place and
776 interconnected on or within a single base material to perform a particular electrical function

777 **integrated passive component**

778 multiple passive components that share a substrate and package

779 Note 1 to entry: Integrated passive components may be housed inside the layers of the primary interconnect
780 substrate, and thus become embedded passive components. Alternately, these components may be on the surface
781 of a separate substrate that is then placed in an enclosure and surface mounted on the primary interconnect
782 substrate, thus become passive arrays or passive networks.

783 **interconnection**

784 joining of electrical devices to complete a circuit

785 **13 J**786 **jisso**

787 total solution for interconnecting, assembling, packaging, mounting, and integrating system
788 design

789 Note 1 to entry: A term from Japanese.

790 **J-leads**

791 preferred surface mount lead form used on PLCCs (Plastic Leaded Chip Carrier), so named
792 because the lead departs the package body near its Z axis centreline, is formed down then
793 rolled under the package

794 Note 1 to entry: Leads so formed are shaped like the letter "J."

795 **junction temperature**

796 temperature of the region of a transition between the p-type and n-type semiconductor
797 material in a transistor or diode element during operation

798 **14 K**799 **known good die**800 **KGD**

801 die-form semiconductor product that provides assurance of equivalent quality and reliability as
802 its conventionally packaged counterparts

803 **known tested die**804 **KTD**

805 die-form semiconductor product functionally verified by probing tests equal to the expected
806 performance of the packaged product, without full quality assurance by supplier(s)

807 Note 1 to entry: The testing requirements are AABUS.

808 **15 L**809 **land grid array**810 **LGA**

811 square package with termination lands located in a grid pattern on the bottom of the package

812 **large-scale integration**813 **LSI**

814 integrated circuit with over 100 gates

815 **lay-up**

816 process of combining one or more innerlayers, and pre-preg or adhesive layer(s) into a
817 lamination package

818 Note 1 to entry: The package may consist of innerlayers, outerlayers and copper foil.

819 **lead frame**

820 metallic portion of the device package on which the integrated circuit die is mounted and
821 connected from the die or dice bonding sites to the structure that becomes the outer leads of
822 the package

823 **lead-free solder**

824 alloy that does not contain more than 0,1 % lead (Pb) by weight and that is used for joining
825 components to substrates or for coating surfaces

826 **leadless chip carrier**

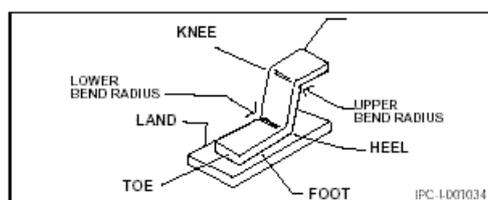
827 a chip carrier whose external connections consist of leads that are around and down the side
828 of the package

829 Note 1 to entry: See also "leadless chip carrier".

830 **leadless surface-mount component**

831 surface-mount component for which external connections consist of leads that are around and
832 down the side of the package

833 SEE: Figure 6.



834

835 **Figure 6 – Leadless surface-mount component – Gull wing shaped lead**

836 Note 1 to entry: See also "leadless surface-mount component".

837 **leadless surface-mount component**838 **leadless component**839 **leadless device**

840 surface-mount component whose external connections consist of metallized terminations that
841 are integral part of the component body

842 Note 1 to entry: See also "leaded surface-mount component".

843 **leakage current**

844 undesired flow of an electrical current at the surface or through the inside of an insulator

845 **line coupling**

846 interaction between two transmission lines that is caused by their mutual inductance and the

847 **load capacitance**

848 capacitance seen by the output of a logic circuit or other signal source

849 **logic circuit**

850 functional digital circuits used to perform computational functions

851 **logic diagram**

852 drawing that depicts the multistate device implementation of logic functions with logic symbols
853 and supplementary notations that show the details of signal flow and control, but not
854 necessarily the point-to-point wiring

855 **logic family**

856 collection of logic functions using the same form of electronic circuit, for example, emitter-
857 coupled logic (ECL), transistor-transistor logic (TTL), complementary metal-oxide
858 semiconductor logic (CMOS)

859 **lot accept number**

860 maximum number of devices which may fail a sample test without causing rejection of the lot

861 **lot reject number**

862 for a sample test, the number of failed devices which will cause lot rejection

863 **lot size**

864 **batch size**

865 collection of units produced in one continuous, uninterrupted fabrication run

866 **luminance**

867 **brightness**

868 quantity defined by the formula

$$869 \quad L_v = \frac{d\Phi_v}{dA \cdot \cos \theta \cdot d\Omega}$$

870 Where:

871 $d\Phi_v$ is the luminous flux transmitted by an elementary beam passing through the given point
872 and propagating in the solid angle $d\Omega$ containing the given direction; dA is the area of a
873 section of that beam containing the given point; θ is the angle between the normal to that
874 section and the direction of the beam

875 unit: $\text{cd} \cdot \text{m}^{-2} = \text{lm} \cdot \text{m}^{-2} \cdot \text{sr}^{-1}$

876 (SOURCE: IEC 60050-845:1987, 845-01-35)

877 **luminous energy**

878 time integral of the luminous flux

879 Note 1 to entry: Luminous energy is measured in lms (lumen second).

880 **luminous flux**

881 a magnitude defined by

$$882 \quad \Phi = K_m \int_0^{\infty} V(\lambda) P(\lambda) d\lambda$$

883 Where:

884 $P(\lambda)$ is the power spectral density radiated by the source at wavelength λ ;

885 $V(\lambda)$ is the spectral luminous efficiency for photopic vision;
886 K_m is a constant

887 Note 1 to entry: In the SI system of units, where $P(\lambda)$ is expressed in watts per metre, the luminous flux Φ is
888 expressed in lumens, and $K_m = 683 \text{ lm/W}$.

889 (SOURCE:IEC 60050-723:1997, 723-08-27)

890 **16 M**

891 **major defect**

892 defect that is likely to result in a failure of a unit or product or that materially reduces its
893 usability for its intended purpose

894 **metal oxide semiconductor**

895 **MOS**

896 fabrication technology, resulting in the creation of FET devices

897 **microcircuit**

898 relatively high density combination of equivalent circuit elements that are interconnected so
899 as to perform as an indivisible electronic circuit component

900 **microcircuit module**

901 combination of microcircuits and discrete components that are interconnected so as to
902 perform as an indivisible circuit assembly

903 **microelectronics**

904 area of electronic technology with, or applied to, the realization of electronic systems from
905 extremely-small electronic elements, devices or parts

906 **microwave integrated circuit**

907 integrated circuit that performs at microwave frequencies

908 **microwaves**

909 radio waves in the frequency range of 1 GHz to 100 GHz

910 Note 1 to entry: The term microwave generally refers to the frequency range where circuits and device
911 interconnects are described as distributed elements instead of lumped elements.

912 **minimally-packaged die**

913 **MPD**

914 die to which some exterior packaging medium and interconnection structure has been added
915 for protection purposes and ease of handling

916 Note 1 to entry: This definition includes such packaging technologies as chip scale packages (CSP) in which the
917 area of the package is not significantly greater than the area of the bare die.

918 **minor defect**

919 defect that is not likely to result in a failure of a unit or product or that does not materially
920 reduce its usability for its intended purpose

921 **mixed component mounting technology**

922 component mounting technology that uses both through-hole and surface-mounting
923 technologies on the same packaging and interconnecting structure

924 **module**

925 separable unit in a packaging scheme

926 **moisture barrier bag**

927 **MBB**

928 bag that is safe from electrostatic discharge (ESD) and is designed to restrict the ingress of
929 water vapour used to package moisture-sensitive devices

930 **molded interconnection device**

931 combination of molded plastic substrate and conductive patterns that provide both the
932 mechanical and electrical functions of an electronic interconnection package

- 933 **monolithic integrated circuit**
934 integrated circuit in the form of a monolithic structure
- 935 **multi-chip module**
936 **MCM**
937 Module that contains two or more die(s) and/or minimally packaged dies
- 938 Note 1 to entry: Also see "hybrid" and "multi-chip package".
- 939 **multi-chip package**
940 **MCP**
941 package that contains two or more die(s) and/or minimally-packaged dies
- 942 Note 1 to entry: Also see "hybrid" and "multi-chip package".
- 943 **multichip module**
944 **MCM**
945 **Multichip integrated circuit**
946 **Multichip microcircuit**
947 microchip module consisting primarily of closely-spaced integrated circuit dies that have a
948 silicon area density of 30 % or more
- 949 **17 N**
- 950 **nominal**
951 design target dimension for a physical characteristic of a product or a feature to which a
952 tolerance may be applied that establishes the limits of variation from the target that are
953 acceptable
- 954 **nominal value**
955 centre value between a minimum and maximum allowance
- 956 **18 O**
- 957 **output vector**
958 set of logic values, either expected or measured, for all output points at a particular test step
959 of a unit under test
- 960 **19 P**
- 961 **package**
962 total assembly which protects one or more electronic components from mechanical,
963 environmental and electrical damage throughout its operational life and which provides means
964 of interconnection
- 965 **package cap**
966 cuplike package cover
- 967 **package cover**
968 cover that encloses the contents in the cavity of a package in the final sealing operation
- 969 **package lid**
970 flat package cover
- 971 **packaging**
972 process of assembling one or more electronic components into a package
- 973 Note 1 to entry: The use of "packaging" as a participle (For example "When packaging ICs into dual-in-line
974 packages ...") is deprecated.
- 975 **packaging and interconnecting assembly**
976 assembly that has components mounted on either or both sides of a packaging and
977 interconnecting structure
- 978 Note 1 to entry: Packaging and interconnecting assembly is a general term.

979 **package cracking**

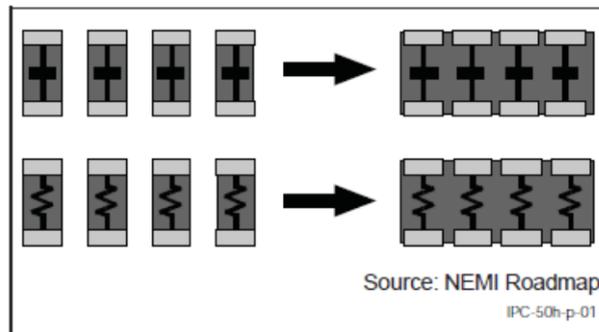
980 cracks in a plastic integrated circuit package caused by stress that results from exposure to
 981 reflow solder temperature

982 Note 1 to entry: These cracks may propagate from the die or die pad to the surface of the package, or only extend
 983 part way to the surface of lead fingers.

984 **passive array**

985 comprises multiple passive components of similar function, which are formed on the surface
 986 of a separate substrate and packaged in a single SMT case and mounted on the primary
 987 interconnect substrate

988 SEE: Figure 7.



989

990

Figure 7 – Passive array

991 Note 1 to entry: Examples include an array of capacitors or resistors.

992 **passive component**

993 <element> discrete electronic device whose basic character does not change while it
 994 processes an applied signal

995 Note 1 to entry: Passive components include components such as resistors, capacitors, and inductors.

996 **passive network**

997 multiple passive components which have more than one function and are formed on the
 998 surface of a separate substrate and packaged in a single SMT case

999 Note 1 to entry: The case is then mounted on the primary interconnected substrate of the system.

1000 Note 2 to entry: Passive networks typically have several internal connections to form simple functions such as
 1001 terminations or filters.

1002 **peak package body temperature**1003 **T_p**

1004 the highest temperature that an individual package body reaches during moisture sensitivity
 1005 level (MSL) classification

1006 **peeling**1007 **perimeter sealing area**

1008 surface on the perimeter of a package cavity that is used as attachment to the package cover

1009 **photometry**

1010 light measurement where the luminous intensity is compared with that of the light source to be
 1011 measured by measurable attenuation

1012 Note 1 to entry: Photometry consists of/comprises visual, physical and photographic photometry. For the visual
 1013 photometry the eye is the receiver.

1014 **pick-up force**

1015 force required to pick up a surface-mount component from its packaging medium for
 1016 placement on a substrate

1017 **pick-up tool**

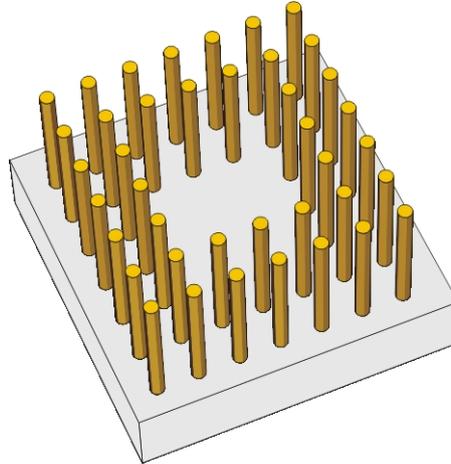
1018 tool used to pick up surface-mount components from a packaging medium for placement on a
 1019 substrate and which may be hand activated or a part of a pick-and-place machine

1020 **pin grid array**

1021 **PGA**

1022 square or rectangular component package with pins protruding from the bottom surface with a
1023 pitch perpendicular to the plane of the package

1024 SEE: Figure 8.



1025

Figure 8 – Pin grid array

1026

1027 **plastic ball grid array**

1028 **PBGA**

1029 polymer based package with interconnects formed of tin-lead solder spheres

1030 Note 1 to entry: The solder interconnects are located in an array area on board side of package.

1031 **plastic device**

1032 semiconductor component wherein the package or encapsulant is plastic

1033 **plastic leaded chip carrier**

1034 **PLCC**

1035 surface-mount family of integrated circuit packages with leads exiting from all four sides of the
1036 package, generally with a 1,27 mm lead-to-lead pitch

1037 **plastic quad flat pack**

1038 **PQFP**

1039 surface-mount family of integrated circuit packages, bounded on all four sides by bumpers,
1040 with leads exiting from all four sides of the package and formed into a “gullwing” lead format

1041 **power dissipation**

1042 energy used by an electronic device in the performance of its function

1043 **power plane inductance**

1044 inductance in response to AC noise, seen on a DC backplane system

1045 **primary side**

1046 **component side**

1047 side of a packaging and interconnecting structure that is defined as such on the master
1048 drawing

1049 Note 1 to entry: It is usually the side that contains the most complex or the highest number of components.

1050 **printed board**

1051 **PB**

1052 **board**

1053 **card**

1054 **circuit card**

1055 **finished board**

1056 completely processed printed circuit and printed wiring configurations

1057 Note 1 to entry: This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex
1058 base materials.

1059 Note 2 to entry: Printed board is a general term.

1060 **printed board assembly**

1061 assembly that uses a printed board for component mounting and interconnecting purposes

1062 Note 1 to entry: Printed board assembly is a general term.

1063 **printed circuit**

1064 **circuit board**

1065 conductive pattern that is composed of printed components, printed wiring, discrete wiring, or
1066 a combination there of, that is formed in a predetermined arrangement on a common base

1067 Note 1 to entry: This is also a generic term that is used to describe a printed board that is produced by any of a
1068 number of techniques.

1069 **printed circuit board**

1070 printed board that provides both point-to-point connections and printed components in a
1071 predetermined arrangement on a common base

1072 Note 1 to entry: See also "printed wiring board".

1073 **printed component**

1074 a part (such as an inductor, resistor, capacitor, or transmission line) that is formed as part of
1075 the conductive pattern of a printed board

1076 **printed component**

1077 <conductive inks> component (For example printed inductor, resistor, capacitor or
1078 transmission line) forming part of the pattern of a printed circuit

1079 **printed contact**

1080 portion of a conductive pattern that serves as one part of a contact system

1081 **printed electronics sheet board**

1082 sheet (board) of forming an electronically functional pattern and/or devices on a large-scale
1083 by printing of conductive materials

1084 Note 1 to entry: Applications of a printed electronics sheet may include sensors of various types including image
1085 and pressure, thin film secondary battery, smart card, RF-IC, etc.

1086 **printed wiring**

1087 conductive pattern that provides point-to-point connections but not printed components in a
1088 predetermined arrangement on a common base

1089 Note 1 to entry: See also "printed circuit".

1090 **printed wiring board**

1091 printed board that provides point-to-point connections but not printed components in a
1092 predetermined arrangement on a common base

1093 Note 1 to entry: See also "printed circuit board".

1094 **printing**

1095 act of reproducing a pattern on a surface by any process

1096 **propagation delay**

1097 time from output to input required for a signal to travel along a transmission line, or the time
1098 required for a logic device to receive an input stimulus, perform its function, and present a
1099 signal at its output

1100 **pulse**

1101 <digital>logic signal that switches from one digital state to the other and back again in a short
1102 period of time, and that remains in the original state for most of the time

1103 **20 Q**

1104 **QFP with bumper**

1105 **BQFP**

1106 QFP package with a guarding bumper

- 1107 **quad flat J-lead**
 1108 **QFJ**
 1109 generic rectangular component package, containing an electronic device, with leads on all
 1110 four sides that are formed in a “J” shape
- 1111 **quad flat no-lead**
 1112 **QFN**
 1113 generic rectangular component package outline wherein the metal pad terminations are
 1114 formed on four sides of the bottom of a package
- 1115 **quad flat pack**
 1116 **QFP**
 1117 **Plastic QFP**
 1118 **PQFP**
 1119 generic square or rectangular component package, containing a semiconductor die, with leads
 1120 on all four sides that are formed in a “gullwing” shape
- 1121 **qualification testing**
 1122 demonstration of the ability to meet all of the requirements specified for a product
- 1123 **quality conformance testing**
 1124 qualification testing that is performed on a regularly scheduled basis in order to demonstrate
 1125 the continued ability of a product to meet all of the quality requirements specified
- 1126 **21 R**
- 1127 **radiant flux**
 1128 power emitted, transmitted or received in the form of radiation
 1129 unit : W
- 1130 (SOURCE:IEC 60050-845:1987, 845-01-24)
- 1131 **radiant intensity**
 1132 **power of source**
 1133 quotient of the radiant flux $d\Phi_e$ leaving the source and propagated in the element of solid
 1134 angle $d\Omega$ containing the given direction, by the element of solid angle
- 1135
$$I_e = \frac{d\Phi_e}{d\Omega}$$
- 1136 unit : W • sr⁻¹
- 1137 (SOURCE:IEC 60050-845:1987, 845-01-30)
- 1138 **radiation**
 1139 <infrared>thermal radiation emitted in the infrared region of the electromagnetic spectrum
- 1140 **radiation**
 1141 <long wave infrared>infrared energy that is radiated at a wavelength that is between 5
 1142 microns and 100 microns
- 1143 **radiation**
 1144 <medium wave infrared>infrared energy that is radiated at a wavelength that is between 2,5
 1145 microns and 5 microns
- 1146 **radiation**
 1147 <re-emitted infrared>portion of thermal energy absorbed by a media that is in turn emitted in
 1148 the infrared portion of the electromagnetic spectrum
- 1149 **radiation**
 1150 **near infrared radiation**
 1151 <short wave infrared>infrared energy that is radiated at a wave length that is between 0,78
 1152 microns and 2,5 microns

- 1153 **radiometry**
1154 measurement of radiation in the optical spectrum
- 1155 Note 1 to entry: This includes infrared (IR), ultraviolet (UV), and visible.
- 1156 **random sample**
1157 set of individuals that is taken from a population in such a way that each possible individual in
1158 the population has an equal chance of being selected
- 1159 **reflection**
1160 <signal propagation> fraction of a propagating signal that is reflected back toward its source
1161 after the signal has encountered a discontinuity in the electrical impedance of the
1162 transmission line on which it is traveling
- 1163 **reflection coefficient**
1164 ratio of the power or voltage of a microwave signal reflected from a load resistance that is
1165 attached to a circuit or transmission line to the power of the incoming signal
- 1166 **relative permittivity**
1167 ϵ_r
1168 ratio of the permittivity of a material to that of free space
- 1169 **reliability**
1170 probability that a component, device, or assembly functions properly for a definite period of
1171 time under the influence of specific environmental and operational conditions
- 1172 **return loss**
1173 level of the reflected signal which is a result of a mismatch between a load and a source
- 1174 Note 1 to entry: It is usually expressed as the ratio of reflected power to incident power in dB.
- 1175 **rigid-flex double-sided printed board**
1176 **flex-rigid double-sided printed board**
1177 flex-rigid printed board with conductive patterns on two sides comprising one conductive
1178 pattern on the flexible base material and the other on the rigid base material
- 1179 (SOURCE:IEC 60050-541:1990, 541-01-17)
- 1180 **rigid-flex printed board**
1181 **flex-rigid printed board**
1182 **flex-rigid printed wiring board**
1183 printed board using a flexible base material and a combination of flexible and rigid base
1184 materials in different areas
- 1185 Note 1 to entry: Both the flexible and the rigid base material bear conductive patterns which are normally
1186 interconnected in the combined area
- 1187 (SOURCE:IEC 60050-541:1990, 541-01-16)
- 1188 **rise time**
1189 the interval of time between the instants at which the instantaneous value of a pulse first
1190 reaches a specified lower value and then a specified upper value
- 1191 Note 1 to entry: Unless otherwise specified, the lower and upper values are fixed at 10 % and 90 % of the pulse
1192 magnitude.
- 1193 (SOURCE:IEC 60050-161:1990, 161-02-05)
- 1194 **22 S**
- 1195 **sampling plan**
1196 statistically derived set of sample sizes, accept numbers, and/or reject number which will
1197 confirm that a given lot of materials meets established AQLs or LTPDs
- 1198 **schematic diagram**
1199 drawing that shows, by means of graphic symbols, the electrical connections, components
1200 and functions of a specific circuit arrangement

- 1201 **screen printing**
1202 **silkscreening**
1203 transferring of an image to a surface by forcing a suitable screen printing ink with a squeegee
1204 through an imaged-screen mesh
- 1205 **secondary side**
1206 tside of a packaging and interconnecting structure which is opposite the primary side
- 1207 Note 1 to entry: It is the same as the "solder side" on printed boards for through-hole mounting technology.
1208 Note 2 to entry: See also "primary side".
- 1209 **section beam**
1210 flanged cylinder onto which yarn is drawn and accumulated from the yarn bobbins or
1211 packages
- 1212 **sectional specification**
1213 **SS**
1214 document that describes the specific requirements pertaining to a portion of a set, family, or
1215 group of products, materials, or services
- 1216 **semiconductor**
1217 solid material, such as silicon, that has a resistivity that is midway between that of a
1218 conductor and of a resistor
- 1219 **semiconductor carrier**
1220 package for semiconductor die
- 1221 **sheet resistance**
1222 electrical resistance of a planar film of a resistive material with uniform thickness as
1223 measured across opposite sides of a unit square pattern
- 1224 Note 1 to entry: Sheet resistance is expressed in ohms per square.
- 1225 **shelf life**
1226 duration of the time interval a raw material or semi-finished product may be stored under
1227 specified conditions without changing any important properties
- 1228 (SOURCE:IEC 60050-212:2010, 212-13-15)
- 1229 **shielding**
1230 <electronic> physical barrier, that is usually electrically conductive, that reduces the
1231 interaction of electric or magnetic fields upon devices, circuits, or portions of circuits
- 1232 **shrink sop**
1233 **SSOP**
1234 family of component packages with four sizes, each having the ability to provide lead pitches
1235 between 0,625 mm (0,002 5 in) and 0,3 mm (0,012 in)
- 1236 **signal**
1237 electrical impulse of a predetermined voltage, current, polarity and pulse form representing
1238 information to be transmitted
- 1239 **signal conductor**
1240 individual conductor that is used to transmit an impressed electrical signal
- 1241 **signal line**
1242 conductor used to transmit a logic signal from one part of a circuit to another
- 1243 **silicon on insulator**
1244 **SOI**
1245 fabrication technology that uses an insulating material as the bulk material instead of silicon,
1246 which may be sapphire (SOS)
- 1247 Note 1 to entry: Silicon on insulator is a general term.

- 1248 **silicon on sapphire**
1249 **SOS**
1250 specific fabrication technology that uses sapphire, a variety of corundum (Al_2O_3), as the bulk
1251 material instead of silicon
- 1252 **single chip package**
1253 **SCP**
1254 integrated circuit package containing only one semiconductor die
- 1255 **single-inline package**
1256 **SIP**
1257 component package with one straight row of pins or wire leads
- 1258 **single-sided assembly**
1259 packaging and interconnecting structure with components mounted only on one side
- 1260 Note 1 to entry: See also "double-sided assembly".
- 1261 **small outline J-lead**
1262 **SOJ**
1263 generic rectangular component package, whose chip cavity or mounting area occupies a
1264 major portion of the package area, with leads on two opposite sides that are formed in a "J"
1265 shape
- 1266 **small outline no-lead**
1267 **SON**
1268 generic rectangular component package outline wherein the metal pad terminations are
1269 formed on two sides of the bottom of the package
- 1270 **small outline package**
1271 **SOP**
1272 generic rectangular component package, whose chip cavity or mounting area occupies a
1273 major portion of the package area, with leads or metal pad surfaces on two opposite sides
- 1274 **solderability**
1275 ability of a metal to be wetted by molten solder
- 1276 **soldering ability**
1277 ability of a specific combination of components to facilitate the formation of a proper solder
1278 joint
- 1279 Note 1 to entry: See "solderability".
- 1280 **solid-tantalum chip component**
1281 capacitor in a leadless package whose dielectric material is solid tantalum
- 1282 **substrate bending test**
1283 test applied to a substrate to determine its resistance to bending and the effects of bending to
1284 the substrate and any components mounted on the substrate
- 1285 **support ring**
1286 **omnibus ring**
1287 ring made of a dielectric material that is used to hold beam leads in place relative to one
1288 another outside of a packaged device
- 1289 **supporting plane**
1290 planar structure that is a part of a packaging and interconnecting structure in order to provide
1291 mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical
1292 characteristics
- 1293 Note 1 to entry: It may be either internal or external to the packaging and interconnecting structure.
1294 Note 2 to entry: See also "constraining core".
- 1295 **system in package**
1296 **SiP**
1297 multi-chip package (MCP) that performs a system function

1298 **23 T**1299 **tape carrier package**1300 **TCP**

1301 semiconductor package that has the TAB connection and is coated by a resin

1302 **termination**1303 end of a conductor that connects the conductor to a terminal, distributing frame, switch or
1304 matrix1305 **thick-film circuit**1306 microcircuit in which passive components of a ceramic-metal composition are formed on base
1307 material by screening and firing1308 **thin film**1309 film, less than 0,1 mm thick, deposited by accretion process, such as vacuum or pyrolytic
1310 deposition1311 **thin-film hybrid circuit**

1312 hybrid circuit with thin-film components and interconnections

1313 Note 1 to entry: See also "hybrid circuit".

1314 **thin-film integrated circuit**

1315 hybrid integrated circuit comprised only of thin-film components and interconnections

1316 Note 1 to entry: See also "hybrid integrated circuit".

1317 **thin QUAD flat pack**1318 **TQFP**

1319 surface-mount family of integrated circuit packages with a thin polymer body

1320 **thin small outline package**1321 **TSOP**1322 package that has the same features as the SOP package except that its thickness is reduced
1323 to 0,8 mm to 1,2 mm1324 **traceability**1325 tracking of the manufacturer at a minimum or the manufacturing process of each element
1326 used in a unit1327 **transmission line**

1328 device for guiding or conducting electromagnetic energy from one point to another

1329 Note 1 to entry: A transmission line consists of two or more parallel conductors each separated by a dielectric.

1330 Note 2 to entry: See also "balanced transmission line," "microstrip" "stripline," and "unbalanced transmission
1331 line."1332 **tri-state**1333 **high-impedance state**1334 high-impedance state of an electronic device that effectively disconnects the device output
1335 from all other circuitry1336 **24 U**1337 **unbalanced transmission line**1338 transmission line that has distributed inductance, capacitance, resistance, and conductance
1339 elements that are not equally distributed between its conductors1340 **uncased device**

1341 component without a package

1342 **unfil**1343 device attached to the loom which automatically winds yarn onto quills from yarn packages
1344 and maintains a supply of quills for the shuttle

1345 **user**

1346 individual, organization, company or agency responsible for the procurement of electrical/
1347 electronic hardware, and having the authority to define the class of equipment and any
1348 variation or restrictions (i.e., the originator/custodian of the contract detailing these
1349 requirements)

1350 **25 V**1351 **very large scale integration**1352 **VLSI**

1353 integrated circuits with more than 80 000 transistors on a single die that are interconnected
1354 with conductors that are 1 micron or less in width

1355 **visible light**

1356 <band> electromagnetic radiation that occurs at wavelengths between 0,39 microns and 0,78
1357 microns

1358 **26 W**1359 **Wafer**1360 **Slice**

1361 slice or a flat disc, either of semiconductor material or of such a material deposited on a
1362 substrate, in which one or more circuits or devices can be processed

1363 (SOURCE:IEC 60050-521:2002, 521-05-29)

1364 **wafer level package**1365 **WLP**

1366 technique of partial encapsulation and protection of die while still on the wafer and before the
1367 wafer is divided into singulated dies

1368 **wafer-level package**

1369 <chip-scale package> A chip-scale package whose size is generally equal to the size of the
1370 semiconductor device it contains and that is formed by processing on a complete wafer rather
1371 than on an individual device.

1372 NOTE 1 Because of the wafer-level processing, the size of a wafer-level package may be defined by finer
1373 dimensions and tighter tolerances than those for a similar non-wafer-level package.

1374 NOTE 2 The package size will change with changes in the size of the die.

1375 **waveguide**

1376 a transmission line consisting of a system of material boundaries or structures for guiding
1377 electromagnetic waves

1378 Note 1 to entry: Common forms of waveguide include metallic tubes, dielectric rods and mixed structures of
1379 conducting and dielectric materials.

1380 (SOURCE:IEC 60050-704:1993, 704-02-06)

1381 **wavelength**

1382 distance in the direction of propagation of a periodic wave between two successive points at
1383 which the phase is the same distance in the direction of propagation of a periodic wave
1384 between two successive points at which the phase is the same. unit: m

1385 Note 1 to entry: The wavelength in a medium is equal to the wavelength in vacuo divided by the refractive index
1386 of the medium. Unless otherwise stated, values of wavelength are generally those in air. The refractive index of
1387 standard air (for spectroscopy : t = 15 °C, p = 101 325 Pa) lies between 1.000 27 and 1.000 29 for visible
1388 radiations.

1389 Note 2 to entry: $\lambda = v/f$, where λ is the wavelength in a medium, v is the phase velocity in that medium, and f the
1390 frequency.

1391 (SOURCE:IEC 60050-845:1987, 845-01-14)

1392 **wire bond**

1393 completed wire connection that provides electrical continuity between the die and a terminal

- 1394 **wire bonding**
1395 microbonding between a die and base material, lead frame, etc.
- 1396 **27 Z**
- 1397 **zigzag in-line package**
1398 package with in-line leads on one side which are arranged in zigzag fashion
- 1399