

# Journal of the Institute of Circuit Technology

Vol.10 No.3 Summer 2017 Issue

<b>Editorial</b>	2
<b>Council Members</b>	2
<b>Membership News</b>	2
<b>Electronics compliance after Brexit – is the mist clearing?</b> <i>Len Pillinger F.Inst.C.T</i>	3-6
<b>Megasound acoustic agitation for enhanced copper electrodeposition in via interconnects</b> <i>Thomas Jones</i>	7-14
Review of :- <b>ICT 43rd Annual Symposium.</b> <b>Dudley,UK,9th May 2017</b> <i>Pete Starkey</i>	15-19
Review of :- <b>“First Year at Chester University”</b> <i>Bill Wilkie</i>	20
<b>ICT Corporate Members</b>	21

## 2016 Events

- 13/14th April **EMPS-7th Electronic Materials and Processes for Space Workshop**  
*Wednesday-Thursday*  
at Portsmouth University  
<http://emps.port.ac.uk/documents.html>
- 1st June **ICT Annual Symposium**  
*Wednesday*  
at M Shed, Bristol  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- 20th September **ICT Hayling Island Seminar**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- 1st December **ICT Harrogate Seminar**  
at the Majestic Hotel,  
Harrogate  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)

## 2017 Events

- 14th March **ICT Evening Seminar and AGM**  
*Tuesday*  
at the Best Western Plus  
Manor Hotel, Meriden  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- 24th-27th April **ICT Annual Foundation Course**  
at Chester University  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- 9th - May **ICT Annual Symposium**  
*Tuesday*  
at the Black Country Museum  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- September **ICT Evening Seminar**  
TBA  
at Hayling Island  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- November **ICT Evening Seminar**  
TBA  
at Harrogate  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)

Vol.10 No.3

This issue is being published at least two weeks early, so that full advantage may be gained from the topicality of the two papers and review, that we are sure Members will find very interesting and informative.

*The Journal* is always trying at all times to keep abreast of the latest developments and technologies, that Members or other people in our industry may have knowledge. Such subjects as new ways of imaging, Including 3D printing. Which must be capable of producing thinner substrates, better connections between layers and flatter more staple PCBs. Possibly using more sophisticated materials for the conductors and insulators.

If you have any thoughts or ideas that you would like to expand, please initially contact the Editor by any of the methods at the bottom of the page. If you choose to use the phone, please remember that he is a deaf old man of 93 years and may not be able to hear you.

*Bruce Routledge*

Editor

---

**Council** Andy Cobby (*Chairman*), Steve Payne (*Deputy Chairman*), Chris Wall (*Treasurer*), William Wilkie  
**Members** (*Membership Secretary & Events*), Bruce Routledge (*the Journal*), Richard Wood-Roe (*Web Site*),  
**2016/7** Martin Goosey, Lynn Houghton, Maurice Hubert, Lawson Lightfoot, Peter Starkey, Francesca Stern, Bob Willis.

---

**Membership** *New members notified by the Membership Secretary*

10407 Mike Fairclough A.Inst.C.T.	10418 Gordon McGaw A.Inst.C.T.
10408 Dan Feery A.Inst.C.T.	10419 Marc Wilkinson A.Inst.C.T.
10409 Kate Pooley A.Inst.C.T.	10420 Adam Fairfield A.Inst.C.T.
10410 Peter Roberts A.Inst.C.T.	10421 Carlos Andre Araujo Ferreria A.Inst.C.T.
10411 Guillaume Jacqmin A.Inst.C.T.	10422 Carlos Daniel Araujo Ferreria A.Inst.C.T.
10412 Denis Albert A.Inst.C.T.	10423 Joao Miguel Leite Oliveira Silva A.Inst.C.T.
10413 Youssef Hamid A.Inst.C.T.	10424 Rui Miguel Lopes Cunha A.Inst.C.T.
10414 Ben Morris A.Inst.C.T.	10425 Sean Cooney A.Inst.C.T.
10415 Garry Brice A.Inst.C.T.	10426 Mike Timmins A.Inst.C.T.
10416 Ethan Stoyale A.Inst.C.T.	
10417 Robert Boldis A.Inst.C.T.	

**Corrections & Clarification**

*It is the policy of the Journal to correct errors in the next issue  
Please send corrections to :-*

*brucer@john lewis.com*

---

*The Journal of the Institute of Circuit Technology is edited by Bruce Routledge on behalf of the  
**Institute of Circuit Technology.***

*4 Burnhams Field, Weston Turville, HP22 5AF. Tel:01296 394 383 E-mail : brucer@john-lewis.com*

---

# Electronics compliance after Brexit – is the mist clearing?

by **Len Pillinger F.Inst.C.T**



**Len Pillinger F.Inst.C.T**

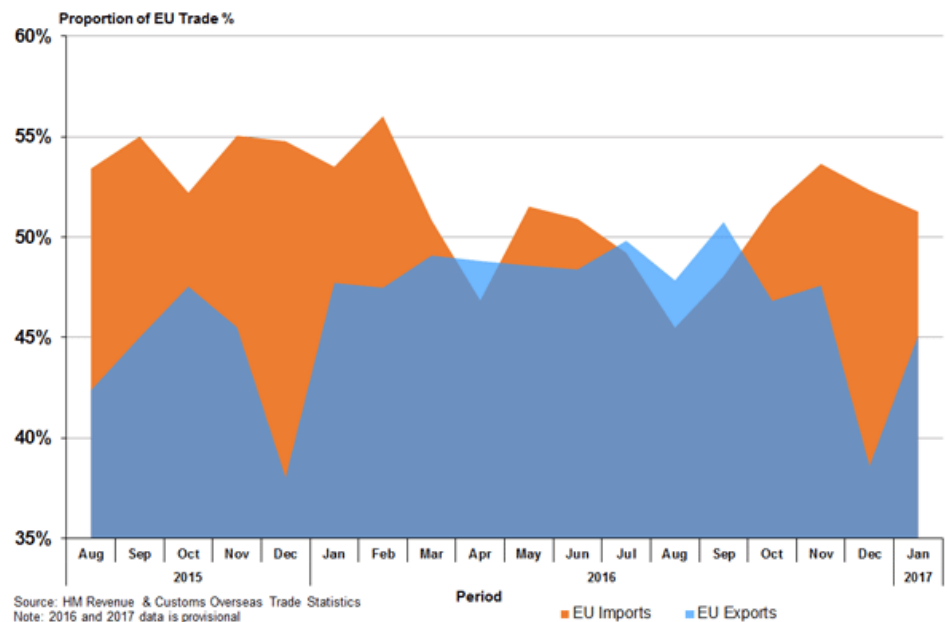
What follows is a series of statements of the obvious. However, Brexit has seen a feast of specious claims, lies, damn lies and dubious statistics. Any prognosis therefore needs to be anchored on the few facts available. For compliance engineers in the electrical / electronics manufacturing section I believe that it is a case of 'keep calm and carry on'.

The **European Economic Community** established the **Single Market** on the 1<sup>st</sup> of January 1993. For quality and compliance engineers in the UK electronics industry this was a considerable upheaval. When I joined the BSI technical committee for printed circuit boards in 1986 the focus was on helping to make some immature EU PCB quality conformance Standards fit for UK use so that mature but conflicting UK Standards could be withdrawn. Higher up the electronics supply chain there was a tranche of product Directives and the CE mark to become familiar with. The benefit was that this provided a single set of requirements throughout the EEC rather than individual country-by-country criteria.

Will leaving the Single Market be a similar upheaval? Hopefully not; but just how much do we know so far?

## ***Single Market; how important to the UK?***

I am one of those annoying fact checkers that needs to find provenance to substantiate what I am told! With claim and counter-claim about UK exports to the EU during the referendum campaign, the HMRC website [https://www.uktradeinfo.com/Statistics/OverseasTradeStatistics/Pages/EU\\_and\\_Non-EU\\_Data.aspx](https://www.uktradeinfo.com/Statistics/OverseasTradeStatistics/Pages/EU_and_Non-EU_Data.aspx) provides data of unimpeachable provenance.



HMRC say that in the 18 months to January 2017 between 38% and 51% of UK exports went into EU Member States. This is presumably value (rather than tonnage) of both goods and services and therefore dependant on exchange rates.

Obviously most UK manufacturers will still be needing to satisfy

EU product legislation in much the same way as any other non-EU exporter.

### ***What about Product Standards?***

It looks as if this will also be a case of 'business as usual'. The PCB fabrication industry makes increasingly greater use of IPC publications. However, equipment manufacturers need to use Harmonised European Standards. These provide a legal 'presumption of conformity' with the 'essential requirements' of EU Product Directives. It is possible to ignore such Standards, but at your own risk and responsibility.

The boring bit: Most British Standards are authored by industry representatives at national committees under the auspices of the International Standards Organisation (ISO) or the International Electrotechnical Commission (IEC). These are recognised by the Committee for European Normalisation (CEN) and in particular CENELEC for the electrical / electronics industry.



CEN and therefore CENELEC, whilst being key to the Single Market, are independent of the EU. BSI's involvement in the development of Standards will not be prejudiced by Brexit.

### ***UK adoption of EU legislation***

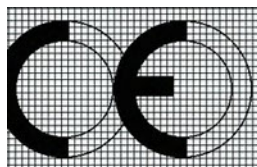
I am writing this during the week that the 'Article 50' letter has been delivered and the 'Great Reform Bill' begins to be debated. During the referendum campaign there was a great deal of heat generated about the degree to which an EU Member State can or cannot make its own laws. The totality of the EU's law and associated court decisions is known as the 'Acqui Communautaire'. Some sources estimate that the wordage covers more than half a million pages of size nine font on A4 paper. Obviously some of this will be adopted by the UK and some discarded. How big a task is this and how long will it take?

To quote from information at [www.parliament.org.uk](http://www.parliament.org.uk) "The House of Commons Library has estimated that 13.2% of UK primary and secondary legislation enacted between 1993 and 2004 (the first decade of the Single Market) was EU related. The review of all EU-related legislation, as well as that which will be transposed by the Great Repeal Bill, makes this potentially one of the largest legislative projects ever undertaken in the UK. It is not yet known when the legislative changes will be made to give effect to any withdrawal agreement made with the EU."

It would appear that any legislative changes needed to support the electronics industry may take some considerable time to enact.

### ***The UK and the CE mark***

Most electronic products offered for sale in the EU are now made on other continents, so manufacturing outside the EU is not an issue. In the vast majority of cases where the CE mark is applied on the basis of self-declaration there is no need for change.



However some products require that a third-party known as a **'Notified Body'** is involved. If the CE mark is accompanied by a number (as below) it has been 'affixed' with the involvement of a Notified Body. These are mostly high risk items such as construction products, medical devices, gas appliances, items used in potentially explosive atmospheres and some radio products. Electronics cuts across all these sectors.



Each Member State has accredited certification and testing bodies which they notify (hence the term) to the EU. In principle a Notified Body has to reside in an EU member State. Where does this leave the 189 UK Notified Bodies and their industry customers in the UK after Brexit? The EU already has seven Memoranda of Understanding with countries such as Canada, Turkey and the USA, so it seems inevitable that the UK will seek similar arrangements. A concern is whether this will receive sufficient priority, given the long list of other tasks. This concern is voiced in the recent House of Commons Library Briefing Paper 7739:

### **3.3 What practical issues could arise as a result of the transposition of EU law?**

Aside from the question of which of those currently directly applicable laws will be kept, there is also the question of how they will be transposed so that they work effectively post-Brexit.

An example of where transposition may give rise to difficulties is when the laws in question make reference to, and depend upon, European Union institutions or agencies. The European Medicines Agency (EMA) is responsible for evaluating medicinal products, and is directly referred to in the relevant EU regulations. Professor Sionaidh Douglas-Scott identifies questions arising from this scenario:

Post Brexit, would the UK continue to accept decisions by a relocated EMA until a new British equivalent had been set up, which could take several years? If there were a British equivalent, there would also have to be arrangements for mutual recognition of UK and EU agency decisions, otherwise applicants would face extra costs of going through two agencies. This may sound technical, but such matters will arise with literally hundreds of EU provisions, requiring thought, time, expertise and cost before the law will be workable.

Whilst medicinal products is given in this example, this concern applies to any industry sector where third-party certification is mandated for CE or similar marking, many of which rely on high reliability electronics.

### ***To conclude***

I have tried to avoid any personal opinions but I draw the following conclusions:

All UK industry sectors will continue using existing familiar EU product requirements.

The UK electronics industry will continue to use and develop the Standards it has always used.

The status of the UK's EU Notified Bodies, whilst not in long-term jeopardy, may suffer a temporary hiatus. Their customers would be wise to liaise closely to ensure continuity of service.

Finally, what kind of silly word is 'Brexit'? According to my passport I live in the 'United Kingdom of Great Britain *and Northern Ireland*'. I imagine that folk in the six counties shout "UKexit" each time they hear Brexit mentioned!

***Len Pillinger F.Inst.C.T***

# Megasound acoustic agitation for enhanced copper electrodeposition in via interconnects

by

*Mr Thomas Jones, Dr David Flynn,  
Prof. Marc P.Y. Desmullie*

*Mr Thomas Jones, Mr Dennis Price,*

**HERIOT  
WATT** *School of Engineering  
& Physical Sciences,  
Heriot-Watt University,  
Edinburgh EH14 4AS  
Scotland, UK*



*Merlin Circuit Technology Ltd.,  
Hawarden Industrial Park,  
Deeside,  
North Wales*

Research Associate  
at Heriot-Watt University



**Mr Thomas Jones**  
*Heriot Watt University and  
Merlin Circuit Technology Ltd.*

Director of the  
Smart Systems Group  
at Heriot-Watt University



**Dr David Flynn**

## 1. Introduction

A Printed Circuit Board (PCB) is populated with a multitude of electro-mechanical components plus various active and passive devices such as transistors, capacitors, inductors and resistors, which enable the functionality and assembly of the PCB. Increasing the density of the components on the surface of a board enables greater functionality and use. A high density (HD) design is desirable for technology high end applications, which includes automotive, aerospace, space, defense, mobile phones, medical, networking, communications, and computer storage [1]

The current trend in PCB markets is low-technology, high-volume demand and is typically supplied by low-cost, large-scale facilities in Southeast Asia, such as China, India and Thailand. High-value, low volume PCB markets are typically supplied by smaller sized facilities in western regions such as North America and Europe, but also economically developed eastern locations such as Japan, South Korea and Taiwan [2] The UK PCB demand typically focuses on this latter market. Manufacturing developments bringing increased capability and cost savings to a factory in the UK would be highly desirable and enable increased market competitiveness.

For more than four years Merlin Circuit Technology Ltd (MCT), in Deeside, North Wales, has been working in collaboration with Heriot-Watt University (HWU), in Edinburgh, Scotland, on a UK government project funded by The Engineering and Physical Sciences Research Council (EPSRC), looking to improve HD PCB manufacturing capability through enhancements to the electrodeposition of copper using high frequency acoustic, applied within a copper plating bath [3-5]. This article outlines some of the key findings from this project.

## 2. High-frequency acoustics applied within manufacture

The introduction of high frequency acoustics – greater than the human hearing range which is typically over 20 kHz – has been used as a manufacturing tool to assist the etchant abilities of wet chemical processes.

Examples include enhancement to the surface treatment of chemically inert materials, by applying 40 kHz ultrasound waves within the permanganate Desmear process used in the electroless copper plating [6] and for the cleaning of silicon wafers for the adhesion of photoresist dry-film [7]. Another application is the enhancement to the streaming of fluidic currents within copper plating baths, which has a use in electrodeposition processes as an assistance to the circulation of electrolyte plating solution in difficult-to-plate regions on the PCB. The resulting use of ultrasonic (US) and megasonic (MS) assisted agitation, leads to increases in the throwing power of the electrolyte bath - its ability to plate into low current density areas with the same thickness as higher current density areas.

Deputy Head of  
Research Institute in  
Signals, Sensors and Systems at  
Heriot - Watt University



**Prof Marc P.Y. Desmullie**

Technical Department at  
Merlin Circuit Technology Ltd.



**Dennis Price**

The introduction of MS agitations within a copper sulphate plating bath has been demonstrated in laboratory trials at HWU to increases in the throwing power of the bath [8]. The advantages outlined in those laboratory-scale trials indicate that the micro features present in PCB interconnects, such as a through-hole via (THV) – a drilled feature which provides electrical connection between a board’s two outer surfaces and inner layers - can be uniformly filled with copper with a feature size of 0.2 mm diameter and diameter-to-depth aspect ratio (ar) 8:1. Also, the uniform filling of a blind via (BV) – a drilled feature smaller than a THV connecting an outer layer with the underlying one, two or three innerlayers - observed on features of diameter 0.1 mm and ar 3:1 [3]. The increased throwing power of the bath due to the MS assisted agitation has demonstrated a potential to manufacture via interconnects with a uniform fill of copper, which is desirable for enhancing thermal transport on a PCB whilst enabling HD interconnection [9]. Increasing the throwing power enables an increased plating performance and via ar, as shown by the 3:1 ar BV which is typically manufactured with a maximum ar of 1.2:1. The outcome of this increased connectivity is illustrated in Table 1. The table shows a PCB schematic of a 26 layer multilayer board fabricated with standard processing – left, and MS-assisted agitation – right, with the THV and BVs indicated by the orange vertical features. A multilayer PCB is constructed by the bonding together of its individual layers by thermally degrading processes. With MS-assisted processing the number of bonding operations is reduced from six to four and the drilling operations reduced from ten to six, which together reduce fabrication costs and overall manufacturing time, and increase the lifetime of the board due to the reduction in high thermal stresses induced during its fabrication. Increasing the lifetime of a PCB is a highly desirable trait for the PCB assembler, who may perform multiple high temperature operations up to 260<sup>o</sup> C, in the reflow soldering of components onto the PCB surface [10].

*Table 1- PCB build comparison of current technology and MOS processing*

26 Layer Build made using standard processing requiring : six bonding and ten drilling operations	26 Layer Build made using MS processing requiring : Four bonding and Six drilling operations

Manufacturing a PCB with the material processing and cost savings outlined would enhance the capability of a PCB fabricator, so a series of investigations were performed looking to scale-up the process from a small-scale laboratory setting – processing in 40 litre tanks at HWU - into a medium scale setting with 500 litre processing tanks at MCT.



### 3. Plating setup and experimental investigations at Merlin

The experimental setup reproduced at MCT was comprised of a 500W Sonosys™ MS acoustic transducer device, submersed within a copper sulphate electroplating bath with a solution provided by Schloetter Ltd, which was SLOTOCOUP CU110, setup for soluble anodes. Before MS-plating the PCBs were processed through a Macdermid™ M-System Omega electroless copper plating line at MCT, depositing 1-2  $\mu\text{m}$  of copper.

When in operation the acoustic transducer was oriented with its active face towards the surface of the PCB, where the features to be plated – THV and BV – were exposed to the oncoming waves. A 2-D schematic of the arrangement is indicated in Fig 1. In the setup one soluble anode was used to the left of the PCB and one transducer was used to the right of the PCB. This setup was applied for the plating trials discussed below.

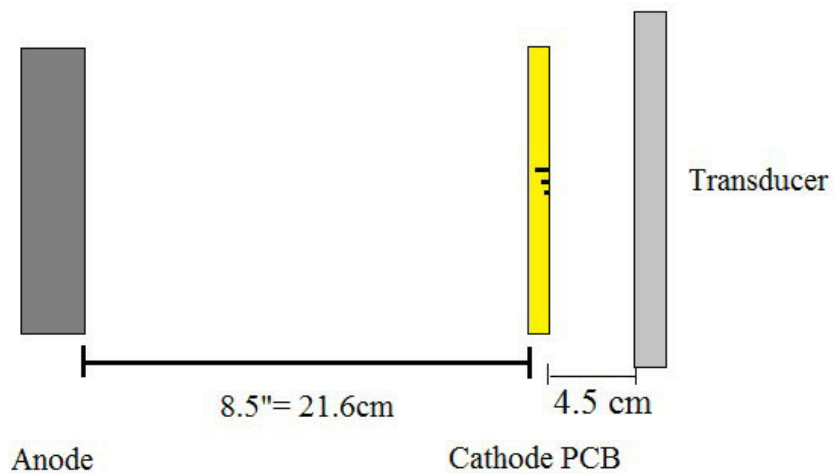


Fig. 1 - Schematic of experimental setup: acoustic transducer, right, PCB, middle, and soluble anode, left. Acoustic agitation applied from right to left onto the PCB surface facing the transducer and into the via interconnects.

A series of investigations were performed looking to investigate:

A) the influence of the MS agitation on the surface finish of the plated copper, from observations using optical microscopes and scanning electron microscopes (SEM), at MCT and HWU, respectively.

B) the ability for the MS acoustic streaming to transport solution down microfeatures, specifically small, 0.15 mm diameter THVs.

C) the ability for the MS acoustic streaming to enhance the amount of copper deposited down small BV interconnects compared to industry standard solution agitation techniques, which include panel movement and bubble agitation.

### 2. Megasound Acoustic Effects observed on the PCB surface

The application of high frequency acoustic agitation during copper electroplating was seen to form periodic features within copper deposited onto substrate surfaces. The periodic features were characterised by regular lines which decreased in distance with increasing frequency [11]. This behaviour was also witnessed in the MS investigations performed at MCT within the deposited copper [4]. A 1.6 mm FR4 PCB was DC plated at 1 A/dm<sup>2</sup> for 1 hour with an acoustic power output of 225 W. After plating the sample was rinsed in D.I. water and dried. A variety of ridge-like features were observed on the plated copper. Shown in Fig 2A is a top-down image of the copper

surface surrounding a tooling hole shown on the top right of the image. Emanating from the hole were concentric ringlets, observed as a dull finish on the PCB. The distance between the ringlets was approximately 0.7 mm, which corresponds to half the acoustic wavelength,  $\lambda$  in the electrolyte solution. The appearance of the periodic ringlets suggested the presence of Rayleigh-type Surface Acoustic Wave (SAW), which have scattered off the PCB and become confined within its surface at fixed locations [12]. The ringlets were characterised by a deposition of large grains with a fine grain region in between. Large grain formation was due possibly to low concentrations of additives at the SAW pressure maxima – these are periodic regions in a SAW where particles or organic molecules attached loosely to a surface will be maximally displaced [13]. The additives might concentrate in the pressure nodal regions – where minimum displacement occurs, increasing in concentration and encouraging a shiny, fine grain finish, shown inbetween the matt ringlets. A matt finish characterised by a large grain structure is more structurally unstable than a fine grain finish, as it demonstrates a greater brittleness and greater susceptibility to fracturing. A PCB has to pass thermal shock testing requirements, for example IPC-6012 standard, where the board is exposed to temperatures up to 288°C. Under these tests a brittle or large grain structuring will be more likely to degrade and cause electrical opens, effectively scrapping the circuit.

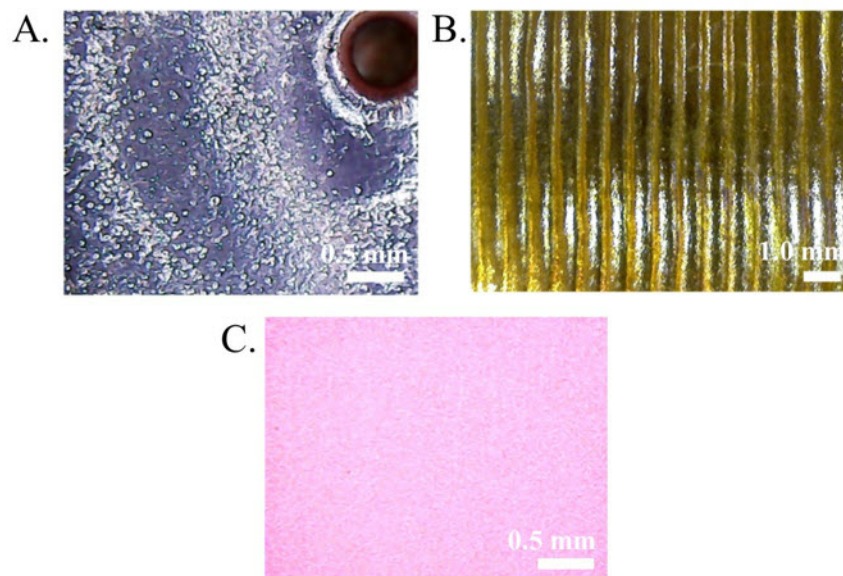


Fig.2 - Optical images of PCB surfaces after MS-plating with 225 W of acoustic power and at DC 1 A/dm<sup>2</sup> for 1 hour, showing after plating  
 A) ringlets emanating from tooling-hole comprised of a large-grain texture and  
 B) copper undulating ridge features.  
 C) shows a typical copper surface after plating under the same current density but with standard bath agitations rather than MS.[4]

Variations in the thickness of the surface finish were also observed within the SAW features. Shown in Fig 2B are copper ridges formed on top of the MS-plated PCB surface. The ridges are again separated by around 0.7 mm and are characterised by peaks and valleys. Ridges occurred on both sides of the board, although during some trials, they would appear greater on one side of a panel rather than the other. This was possibly because of the interplay between the absorption and transmission of the wave through the PCB. The ridge orientation was typically vertical to the orientation of the board in the bath, and

changes to the angle of incidence of the acoustic waves altered accordingly their positions and orientation across the surface. The ridges induced a variation of 20  $\mu\text{m}$  in plating uniformity as measured from cross-sections. This variation is large and could produce a manufacturing difficulty when attempting to keep within a customer's specification for copper thickness. A typical copper surface is indicated in Fig 2C highlighting more ideal copper plating behaviour, which is characterised by high uniformity in height and grain structure.

### 3. Through-Hole Via (THV) plating outcome

Plating within a 500 L tank displays different acoustic reflections and characteristics than plating within a smaller 40 L tank, due to the standing waves and acoustic streaming currents set up within the bath [14]. An experiment was performed to observe if the changes in acoustic conditions in the new bath, due to bath size and fluid flow in the tank at MCT, would still enable electrolyte replenishment down small via interconnects [5]. Plating was performed on a 1 mm thick, FR4 PCB which contained drilled THVs of diameter approximately 0.15 mm and  $ar$  5.7:1. 450 W of MS agitation was applied to the board with the transducer setup as in Fig 1. The board was DC plated at 0.5 A/dm<sup>2</sup> for a duration of 16 hours. Displayed in Fig 3 are the plating results for with MS agitation during the plating and without any agitation what-so-ever, shown in A) and B) respectively. A thicker deposit is clearly highlighted down the MS plated THV, which show that the changes in acoustic conditions due to operating within the new plating tank - such as convective fluid motions and the acoustic reflections off the walls of the tank - did not interfere with the MS plating performance and that fluid transport down the THV was possible, enabling a higher throwing power.

This investigation provided evidence that microfluidic motions induced by the MS acoustic streaming were sufficient to enable electrolyte to be replenished and copper deposited. A plating investigation was then performed to look at how the replenishment of electrolyte by MS compared to the standard processing techniques used in plating. This investigation is discussed next.

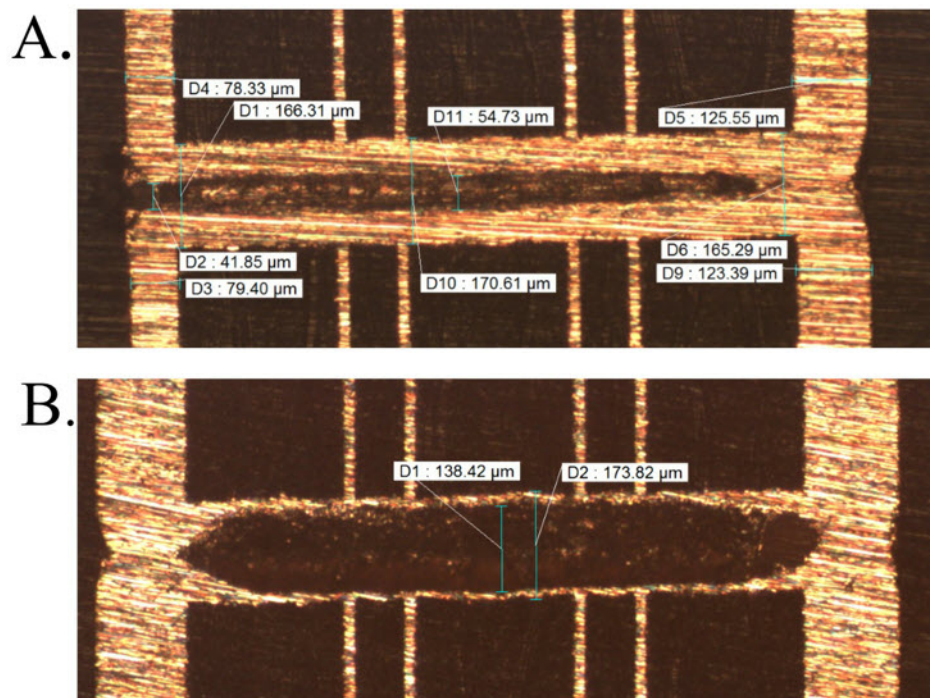


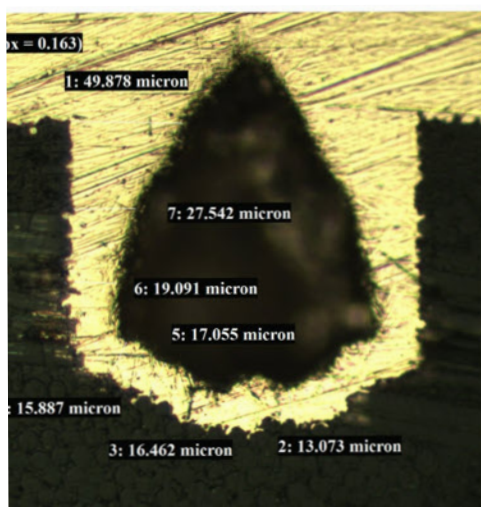
Fig. 3 - Plating performance witnessed down through - hole vias of diameter approximately 0.15 mm,  $ar = 5.7 : 1$ , DC plated at 0.5 A/dm<sup>2</sup> for a duration of 16 hours showing :-  
A) with 450 W of MS and B) without any agitation.[5]

#### 4. Blind-Via (BV) plating enhancement

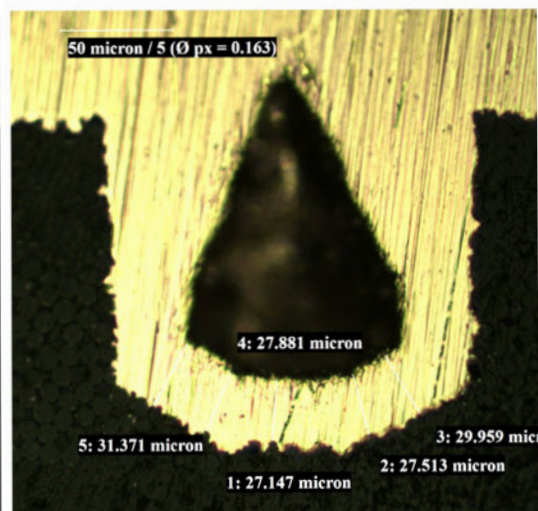
The standard agitations applied in PCB manufacture are the movement of the PCB in solution at a rate of 3 cm/s and the application of bubbles into the solution by a sparge pipe. The action of these two agitations serves as a method of replenishing depleted electrolyte within the microvia features on a board and enables the bath to display a high throwing power, suitable for the electrodeposition of copper. A plating experiment was performed on a 1.6 mm thick FR4 PCB drilled with 0.15 mm diameter *ar* 1:1 BVs, looking to observe the copper plating outcome in response to applying different bath agitations alongside the MS. The acoustic transducer was set up as indicated in Fig 1, and the PCBs were plated with the SLOTOCOUN-CU1 10 plating solution. The plating solution was not configured for via filling and so it was not expected from the plating trials that a uniform filling of Cu would be observed.

Fig 4 shows PCBs plated for 12 hours under pulse-reverse - with a forwards/reverse current density of 1:3 A/dm<sup>2</sup> and with differing bath agitations showing, A) no agitation what - so - ever, B) panel movement and bubbles and C) 450 W MS agitation. The results show clearly that with MS-assisted plating the copper thickness was the greatest. As expected a void was formed in the middle of the via due to the non-filling copper plating properties of the used solution. Regardless, the plated result shows that with MS agitation, greater volumes of electrolyte can be transported and the concentration replenished within the BV over the plated duration, increasing the throwing power of the bath.

Plating with no agitation



Plating with standard agitation — panel movement and bubbles



< Plating with 450W MS agitation

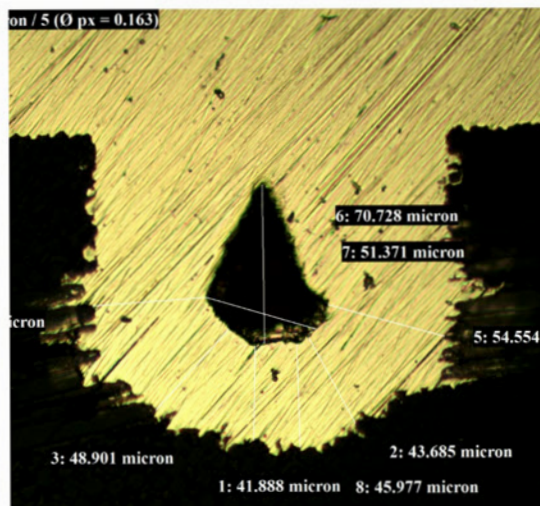


Fig. 4 -Microsections of blind vias 0.15 mm diameter *ar* 1:1, plated with reverse-pulse at 1:3 A/dm<sup>2</sup> for 12 hours, showing results for processing with different electrolyte solution agitation

## 5. Conclusions

A range of plating investigations were performed characterising the plating performance when applying high frequency 1 MHz acoustic agitation to improve the throwing power of a copper sulphate electroplating bath. Observations were made of a surface artefact unique to MS plating which was characterised by an increase in the copper grain size and reduction in plated uniformity. These effects were detrimental to PCB fabrication. Further studies into MS plating using an acoustic transducer, which varies the phase of the outputting wave, may be able to reduce the appearance of these features, whilst maintaining the desired acoustic streaming properties [15].

When electroplating within a 500 L tank in a manufacturing setting the acoustic streaming currents produced by the 1 MHz acoustic wave were shown to transport electrolyte down microscale features in a THV. This confirmed the throwing power of the MS agitations and led to further investigations, which showed that throwing power was higher than the standard bath agitations when plating down BVs. The results obtained show however that considerable development steps are still required to bring MS-assisted plating up to a working standard procedure for implementation into PCB manufacture.

A particular issue in achieving high *ar* plating down BVs – *ar* larger than 1.2:1 – is the lack of a sufficient copper seed layer provided by an electroless copper process. This is because of the difficulty in introducing fresh electrolyte solution into the microscaled regions, due to the effective viscous forces of the fluid medium preventing electrolyte flow. It is the opinion of the author that, using the increased agitation ability of the MS streaming currents, it may be possible to enhance deposition during electroless copper plating, paving the way to further processing developments in the formation of high *ar* BVs.

## Bibliography

1. Technavio *Global Printed circuit Board Market 2016 - 2017*.SKU:IRTNTR8157, 2016.
2. KPCA *Korea PCB Industry*.
3. N. Strusevich, et al., *Electroplating for high aspect ratio vias in PCB manufacturing : enhancement capabilities of acoustic streaming*. Springer Verlag, Journal of Advanced Manufacturing, 2013(1): p. 211-217.
4. T.D.A. Jones, et al., *Megasonic Assisted Electroplated copper Topographies and Acoustic Artefacts*. Circuit World, 2016. **42**(3): p.127 -140.
5. T.D.A. Jones, D. Flynn, and M.P.Y. Desmulliez. *Megasound Acoustic Surface Treatment Process in the Printed Circuit Board Industry*. In *Design, test, Integration & Packaging of MEMS/MOEMS (DTIP)*. 2016. Budapest: IEEE.
6. A.J. Cobley, L.E., M.Goosey, R.Kellner, T.J.Mason, *Initial studies into the use of ultrasound to reduce process temperatures and chemical usage in the PCB desmear process*. Circuit World, Emerald Publishers, 2011. **37**(1): p. 1-9.
7. Keswani, M., et al., *Megasonic cleaning of wafers in electrolyte solutions: Possible role of electro-acoustic and cavitation effects*. Elsevier, Journal of Microelectronic Engineering 2009. **89**: p. 132 -139.

8. S. Costello, et al., *Electrodeposition of copper into high aspect ratio PCB micro-via using megasonic agitation*. Springer Verlag, Journal of Microsystems Technology, 2013: p. 1-8.
9. S.P. Gurrum, et al. *Generic Thermal Analysis for Phone and Tablet Systems. in 62nd Electronic Components and Technology Conference (ECTC)*. 2012. IEEE.
10. Wood, E.R., *Printed Circuit Board Reflow by Vapour Phase Heating*. Circuit World, 1983. **10**(1): p. 26 - 27.
11. Simpson, R.J., *An Effect of Ultrasonic Standing Waves on Electrodeposition*. *Nature*, 1965. **207**(4993): p. 186.
12. Rienstra, S.W. and A. Hirschberg, IWDE 92-06: *An Introduction to Acoustics*. IWDE 92-06. 2013: Eindhoven University of Technology. 1-296.
13. Biryukov, S.V., et al., *Surface Acoustic Waves in Inhomogeneous Media*. 2012: Springer Berlin Heidelberg.
14. Feng, K., L. Yuanyuan, and M. Cheng, *Numerical analysis of the transportation characteristics of a self-running sliding stage based on near-field acoustic levitation*. Acoustical Society of America, 2015. **136**(6): p. 3723 - 3732.
15. Tang, S.C. and G.T. Clement, *Standing-Wave Suppression for Transcranial Ultrasound by Random Modulation*. IEEE Transactions on Biomedical Engineering, 2010. **57**(1): p. 203 - 205.

## Institute of Circuit Technology 43<sup>rd</sup> Annual Symposium. Dudley, UK, 9<sup>th</sup> May 2017

by **Pete Starkey**



**ICT Chairman  
Dr Andy Cobley**



**ICT Technical Director  
Bill Wilkie**



**Ventec Director of OEM  
Technology  
Martin Cotton**

Time marches on and change is inevitable. Here we are anticipating the consequences of a Fourth Industrial Revolution - new technologies are blurring the lines between physical, digital and biological worlds, with the potential to fundamentally alter the way we live, work, and relate to one another. But where and when did the original industrial revolution begin? Look back 300 years, to the blast furnaces and forges of the midlands of England - the Black Country - where innovation, entrepreneurial and manufacturing skills created the world's first industrial landscape. The Black Country Living Museum, which tells the story of that revolution, was venue for the 43<sup>rd</sup> Annual Symposium of the Institute of Circuit Technology.

ICT Chairman **Dr Andy Cobley** welcomed an enthusiastic gathering of PCB professionals to network with their peers whilst enjoying an outstanding symposium programme, this year focused on aspects of design and its impact on PCB manufacturability and reliability.

The keynote presenter, introduced by ICT Technical Director **Bill Wilkie**, was Ventec Director of OEM Technology **Martin Cotton**, *celebrating his 50 years in PCB design.*

Cotton held the attention of the audience for over an hour with an enthralling and action-packed account of his life and career, from modest beginnings in 1951 in north-west London, with an education disrupted by re-location, through the 50 years since his first PCB layout as an apprentice in 1967, to his present-day mission to use the knowledge and experience gained during that half-century to guide OEM customers in selecting and specifying their substrate materials so that product performance and functionality can be optimised whilst maximising manufacturability and cost-effectiveness.

With a series of interesting and often highly amusing anecdotes, he acknowledged the people who had influenced his career and recounted many examples of design challenges he had encountered and overcome, and some of the significant innovations he had introduced, one of the most notable being the principle of "max copper", with particular reference to the IBM P/S2-30 personal computer in the mid-late 1980s.

He re-laid the 4-layer main board as a double-sided and re-panelised it for 2-up manufacture. And all of the redundant space was occupied by a copper ground with no electrically isolated slivers. This resulted in enhanced electrical performance and improved flatness and dimensional stability, as well as reducing the amount of copper to be etched. Cotton had to be innovative in developing a technique for incorporating "max copper", because it was beyond the scope of the CAD systems of the time, and he used a CAM system and "negative data" to achieve it. "Max copper" is a feature of most current designs but, regrettably, Cotton had omitted to patent the concept.

Turning to present-day design challenges, Cotton focused on new-generation high-speed materials and discussed how an understanding of the "impedance triangle" could help designers avoid making controlled-impedance lines narrower than necessary and mitigate some of the consequential effects on trace resistance and insertion loss.



**Senior Market Development  
Manager with Mentor  
Graphics  
Michael Ford**

As a presenter, Martin Cotton is a hard act to follow. But the ICT was privileged to welcome **Michael Ford**, Senior Market Development Manager with Mentor Graphics, who gave an attention-grabbing and thought-provoking performance with his analysis of the essential role of DFM in new product introduction.

He began by considering issues involved in the transition from “Industry 3.0” to “Industry 4.0”, including the automation of automated processes, the computerisation of human decision-making and optimisation based on the live environment, and the significance of these issues in a “lean” context. “Lean” was the mind-set of not doing anything you didn’t need to do, and when you did do something, doing it right-first-time without any waste.

Ford explained that the traditional electronic product ecosystem was a cycle that started and ended with market analysis: create the opportunity, design the product, lay-out the PCB, fabricate the PCB, source the components, assemble, test, ship and distribute. It was in the distribution stage of the value chain where most of the costs lay: assembly cost was trivial in comparison. So if, for example, smart phones were manufactured in Germany, they would cost more to make but less to distribute. But PCB design was the most critical step in the cycle, since it had an impact at every subsequent stage of the cycle, and could ultimately be responsible for missed market opportunities and loss of confidence in the product. And although simple design-rule checking would catch obvious violations, it could miss many issues which might not become apparent until further downstream – manufacture, test or, worst case, failure in the market. Therefore, more intelligent design analysis tools were vital in supporting a successful NPI process.

Does my PCB work for manufacturing? With meaningful illustrations and examples, Ford reviewed a series of design issues that could reduce yield and reliability and incur extra cost in PCB fabrication and assembly processes, describing how designs were analysed for manufacturability and how panels were created to optimise yield and material utilisation in both fabrication and assembly. Use of the right DfX (Design for Excellence) tools in the product ecocycle between PCB layout and PCB fabrication gave the OEM designer the opportunity to improve the design and the EMS provider the facility to expose concerns, as well as enabling direct data input into production tooling. In the lean manufacturing environment, these software solutions helped avoid design re-spins and reduced time to production, with fewer manufacturing problems, higher yields and improved product reliability. And as Industry 4.0 progressed, they resolved many of the issues constraining the traditional product ecosystem, giving the added flexibility to make on-shoring a competitive option.



**Joan Tourné**  
NextGin Technology

It’s not often we see a radical development in PCB interconnection technology, but **Joan Tourné** from NextGin Technology gave an insight into VeCS, a proven alternative approach to Z-axis interconnection which is attracting great interest from OEM designers.

He explained that the major limitation of established HDI technologies was the density of vertical interconnections that could be achieved without going through many stages of sequential build-up - an expensive solution. “Why carry on making things smaller – why not make them easier?” In the VeCS approach, the plated hole was replaced by a vertical trace or half-cylinder, enabling the opportunity to create more vertical connections per unit area as well as freeing up space for routing conductors. And the vertical conductors could connect to multiple internal layers as required. Additional benefits were improved signal integrity and the absence of paths for CAF.

How was this achieved, and was special equipment necessary? Tourné explained that the basic procedure was to form a slot by a



conventional routing operation, and metallise and electroplate it by standard PCB processes, then to drill into the plated slot with a larger diameter drill bit to remove the copper from the areas between the desired vertical conductors. Tool manufacturers could supply router bits designed to minimise burring, and drill-smear problems were avoided because in principle the tool was not withdrawn from the hole it had just cut but was traversed along the slot. Moreover, plating blind slots was more straightforward than plating blind holes of similar diameter and aspect ratio because of better solution penetration and less gas entrapment. So the technology was applicable to any multilayer fabrication facility, with no capital investment required.

Cost savings were realised as a result of reduced layer count for a given interconnection density. If necessary VeCS design features could be incorporated locally on otherwise conventional layouts, for example to overcome fan-out problems under fine-pitch array packages. A further benefit of the VeCS principle was less disruption of internal planes, again improving signal integrity.

VeCS designs were being evaluated by leading OEMs, in cooperation with selected fabricators and assemblers, and EDA vendors were beginning to incorporate VeCS layout capability into their CAD systems.

No visit to the Black Country Museum would be complete without a visit to Hobbs Fish and Chip Shop in the museum's own High Street. Traditionally cooked in beef dripping and served in newspaper, the lunch-time meal eaten standing in the street gave delegates an authentic taste of the past before returning to the conference room for the afternoon session.

Always eagerly awaited at ICT symposia is market analyst **Francesca Stern's** overview of the global PCB and electronics industries.

She summarised trends in electronics production world-wide, then individually for Europe, USA, Japan and China. Likewise, trends in PCB production in Europe, USA, Japan, China/Taiwan and Korea. UK PCB production had shown reasonable growth so far in 2017, but she believed it had now reached a peak and would decline as the year went on, with a further decline in 2018.

The market for PCBs in the UK was increasing slightly, but would flatten in 2018 although there would still be a net import. Her figures did not take into account increasing material costs, partly due to exchange rates and partly to supply chain issues.

She forecast that European PCB production would peak in 2017 and show slightly negative growth in 2018. The USA would show no growth in PCB production in 2017, but she expected some positive trends in 2018. China and Taiwan were still doing quite well if flex and rigid figures were combined, but the substantial growth was in flex. And Japan was not forecast to see growth any time soon.

Back to the design theme, and specifically to considerations of signal integrity in high-speed designs. **Neil Chamberlain**, Signal Integrity Product Manager with Polar Instruments explored the real-world effect of copper surface roughness on insertion loss, and how it could be quantified as a mathematical parameter in a transmission-line field solver

He explained that whereas DC current was carried uniformly through the cross-sectional area of a conductor, AC currents at frequencies of 10MHz and more were carried mainly in the outer skin of the conductor. As conductors became smaller, the skin effect became more significant, and at lower frequencies.



**Francesca Stern**  
Market Analyst



**Neil Chamberlain**  
Signal Integrity Product Manager  
Polar Instruments

“What’s the relationship between frequency and impedance? There isn’t one! But at high frequencies, dielectric loss is the issue.”

Copper foils used in PCB fabrication were deliberately roughened, either electrolytically or chemically, to promote their adhesion to laminating resins. Although “low-profile” and “ultra-low profile” foils were available, they still had some degree of surface roughness and this had a significant influence on skin effect and hence on insertion loss.

PCB designers and pre-production engineers used field solvers for accurate modelling of frequency-dependent PCB transmission lines, to help in choosing appropriate design rules and material parameters. “All models are wrong, but some are useful” was an often-used phrase in the high-speed design community. Chamberlain stressed that effective modelling relied on meaningful input data, and that methods for calculating insertion losses needed to take surface roughness into account.

But how could it be measured and assigned a numerical value? Methods based on mechanically measuring the equivalent number and depth of scratches on conductor surfaces had been used historically, but these were of limited usefulness and only valid for low frequencies. The method proposed by Huray visualised conductor surface topography in terms of pyramids of snowballs and calculated power lost in terms of skin depth and the number and distribution of snowballs in unit area.

Simulations had been conducted using different ball radii, and a single effective ball radius had been used to simplify the formula for practical use.



**Dennis Price**

**Dennis Price** pretended to retire from the industry a couple of years ago, but evidently couldn’t stay away! Recognised and respected for a no-nonsense, common-sense approach, backed by a lifetime of experience, he gave a PCB fabricator’s perspective on Design for Manufacture, which exemplified many of the issues raised in Michael Ford’s earlier presentation.

Acknowledging the range of knowledge, expertise and competence required to be a good PCB layout engineer, amongst them experience of electronics theory, electronic components, circuit diagrams, materials science, PCB fabrication, assembly and test, engineering drawings, engineering specifications, thermal issues, safety rules and regulations and so on, Price described some of the challenges the PCB manufacturing engineer had to address on receipt of the data package.

He discussed the relative cost and yield factors associated with a range of HDI structures, what laminates were specified, and were they the best choice in terms of performance, reliability, availability and cost-effectiveness, the decisions to be made in determining multilayer stack-ups for impedance-controlled designs, and the importance of meaningful fabrication drawings. So much information - and this was in addition to the checking-out of the PCB layout data! He commented that whatever software tools the PCB designer might have used to check his design before forwarding to the PCB fabricator, the fabricator would always run his own DFM checks against his manufacturing capability and resolve any violations or ambiguities before releasing the job for manufacture.

What sort of design features could result in manufacturability problems and potential yield loss? Price showed a whole catalogue of actual examples: drawn features and planes, poor copper distribution and its consequences on plating uniformity, flatness and dimensional stability, poor via hole positioning, via hole in pad issues, component ident on solder joint pads, auto-routing errors and un-terminated tracks,

copper slivers and cross-hatch issues, same net spacing violations. And most of these could have been identified and corrected at the design stage with the sort of DfX tools that Michael Ford had described.

Bill Wilkie brought an extremely enjoyable and informative Annual Symposium to a conclusion, thanked Ventec for their sponsorship of the event and invited Martin Cotton to make the closing remarks. Cotton responded philosophically with some thoughts based on Einstein's "Circle of Knowledge", which could realistically be applied to printed circuit design and manufacture. Inside the circle was knowledge, outside was ignorance, and the interface between the two was the domain of the enquiring mind. The larger the circle, the larger the interface between knowledge and ignorance. The more that was known, the more was unknown, and the more answers you got the more questions were needed. In Cotton's words: "Ignorance is bliss: if you know nothing, there's nothing to learn!"

I am once again indebted to Alun Morgan for kindly allowing me to use his photographs

Pete Starkey  
I-Connect007  
May 2017

### ***Glossary***

<i>Abbreviation</i>	<i>Interpretation</i>
CAD	Computer Aided Design
CAF	Conductive Anodic Filamentation
CAM	Computer Aided Manufacture
DFM	Design for Manufacture
DfX	Design for Excellence
EMS	Electronics Manufacturing Service
HDI	High Density Interconnect
IBM	International Business Machines
NPI	New Product Introduction
OEM	Original Equipment Manufacturer
VeCS	Vertical Conductive Structures

## **ICT Annual Foundation Course "First Year at Chester University"**

by **Bill Wilkie**

---

Our Annual Foundation Course began as the Basic Course in PCB Manufacture in Galashiels in 1980 and has only moved once before, to Loughborough University in 2005, so it was with some trepidation that we chose to relocate to Chester University this year. Pivotal to the move was an offer from Neil Martin, Merlin Group Chairman to host the first day at their Deeside training room, with a facility tour scheduled for the Monday afternoon.

Finding your way around a new University Campus for the first time can be exhaustive, but fortunately, Chester is small by university standards and all the delegates found their way to the campus and the lecture/breakout rooms – as did all the lecturers!

We had twenty one delegates on the 2017 course, four from Portugal, two from Luxembourg and the rest from the UK. As, usual, the vast majority (seventeen) were from fabricator companies, with two from a circuit foil company, a PhD student from Loughborough and a fully-fledged designer, who more than made his mark at each question time!

The get-together Dinner has always been a feature of the course, paving the way for easy discourse for the rest of the week and we were fortunate to be able to hold it in the Senate House, a private dining room in the older part of the University, which made for a memorable evening.

Loughborough has a huge campus, so all activity is centred there, but the halls of residence this year were out with the campus and adjacent to the city walls, enabling delegates to take in the culture of the old city in the evenings. We are there to learn, however and we were fortunate to have an outstanding set of modern lecture theatre and breakout rooms, which makes it easy to absorb the information from seventeen of the best presenters available in our Industry.

**Bill Wilkie**

*Director, Membership Secretary & Events*

## Corporate Members of The Institute of Circuit Technology    June 2017

<i>Organisation</i>	<i>Address</i>	<i>Communication</i>
<b>Adeon Technologies BV</b>	Weidehek 26,A1 4824 AS Breda, The Netherlands	+31 (0) 76-5425059 <a href="http://www.adeon.nl">www.adeon.nl</a>
<b>ALR Services Ltd.</b>	Unit 9 Thame Business Park ,A1 Thame, Oxon OX9 3XA	01844 217 487 <a href="http://www.alrpcbs.co.uk">www.alrpcbs.co.uk</a>
<b>Anglia Circuits Ltd.</b>	Burrel Road, St.Ives, Huntingdon PE27 3LB	01480 467 770 <a href="http://www.angliacircuits.com">www.angliacircuits.com</a>
<b>Atotech UK Ltd.</b>	William Street, West Bromwich. B70 0BE	0121 606 7777 <a href="http://www.atotech.com">www.atotech.com</a>
<b>CCE Europe</b>	Wharton Ind. Est., Nat Lane, Winsford CW7 3BS	01606 861 155 <a href="http://www.ccee.co.uk">www.ccee.co.uk</a>
<b>ECS Circuits Ltd.</b>	Unit B7, Centrepoint Business Park, Oak Road, Dublin 12, Ireland	+353-(0)1-456 4855 <a href="http://www.ecscircuits.com">www.ecscircuits.com</a>
<b>Electra Polymers Ltd.</b>	Roughway Mill, Dunks Green, Tonbridge TN11 9SG	01732 811 118 <a href="http://www.electrapolymers.com">www.electrapolymers.com</a>
<b>The Eurotech Group</b>	Salterton Industrial Estate, Salterton Road Exmouth EX8 4RZ	01395 280 100 <a href="http://www.eurotech-group.co.uk">www.eurotech-group.co.uk</a>
<b>Exception PCB Solutions</b>	Alexandra Way, Ashchurch Business Centre, Tewkesbury, Gloucestershire. GL20 8NB	01684 292 448 <a href="mailto:wwwinfo@exceptionpcbsolutioncom">wwwinfo@exceptionpcbsolutioncom</a>
<b>Merlin PCB Group</b> <i>(was Falcon Group)</i>	Hawarden Industrial Park, Manor Ln, Deeside, Flintshire, North Wales, CH5 3QZ	01244 520510 <a href="http://www.merlinpcbgroup.com">www.merlinpcbgroup.com</a>
<b>Faraday Printed Circuits Ltd</b>	15-19 Faraday Close, Pattinson North Ind. Est., Washington. NE38 8QJ	01914 153 350 <a href="http://www.faraday-circuits.co.uk">www.faraday-circuits.co.uk</a>
<b>Graphic plc</b>	Down End, Lords Meadow Ind. Est., Crediton EX17 1HN	01363 774 874 <a href="http://www.graphic.plc.uk">www.graphic.plc.uk</a>
<b>GSPK (TCL Group)</b>	Knaresborough Technology Park, Manse Lane Knaresborough HG5 8LF	01423 798 740 <a href="http://www.gspkcircuits.ltd.uk">www.gspkcircuits.ltd.uk</a>
<b>Invotec Group Ltd</b>	Hedging Lane, Dosthill , Tamworth B77 5HH	01827 263 000 <a href="http://www.invotecgroup.com">www.invotecgroup.com</a>
<b>PMD (UK) Ltd.</b>	Broad Lane, Coventry CV5 7AY	02476 466 691 <a href="mailto:sales@pmdgroup.co.uk">sales@pmdgroup.co.uk</a>
<b>Rainbow Technology Systems</b>	40 Kelvin Avenue, Hillington Park Glasgow G52 4LT	01418 923 320 <a href="http://www.rainbow-technology.com">www.rainbow-technology.com</a>
<b>Spirit Circuits</b>	22-24 Aston Road, Waterlooville, Hampshire PO7 7XJ	02392 243 000 <a href="mailto:info@spiritcircuits.com">info@spiritcircuits.com</a>
<b>Stevenage Circuits Ltd</b>	Caxton Way, Stevenage. SG1 2DF	01438 751 800 <a href="http://www.stevenagecircuits.co.uk">www.stevenagecircuits.co.uk</a>
<b>Ventec Europe</b>	1 Trojan Business Centre, Tachbrook Park Estate Leamington Spa CV34 6RH	01926 889 822 <a href="http://www.ventec-europe.com">www.ventec-europe.com</a>
<b>Zot Engineering Ltd</b>	Inveresk Industrial Park Musselburgh, B19 EH21 7UQ	0131-653-6834 <a href="mailto:www.data@zot.co.uk">www.data@zot.co.uk</a>