Journal of the Institute of Circuit Technology

2009 Events

21st January	*A ~ Z of Lead-Free Reliability, Smart Group, NPL, Teddington*
3rd February	18.00 Evening Seminar - 3 Papers around Laminates. Pike and Eel at St Ives, Cambridgeshire. Supported by Anglia Circuits
12 - 13th February	*EIPC Winter Conference, Amsterdam*
3rd March	17.00 Evening Seminar, Devonport Hotel, Darlington.
18th March	12.00 Council Meeting London Canal Museum
24th March	*PCB Inspection & Quality Assessment ITRI innovation , St Albans*
25th March	*Troubleshooting Your Assembly Yields ITRI innovation , St Albans*
30th March – 2nd April	Annual Foundation Course , Loughborough University
22nd April	*Step by Step Electronics Failure Analysis ITRI innovation , St Albans*
28th April	*SMART Group, PCB Materials+Finishes - What Assemblers Should Know, The White Swan - Arundel*
5 - 7th May	*CWIEME Berlin 2009 - Electrical Insulation Materials, Electromagnetic Coil, Electric Motor, Transformer Manufacture & Repair.*
4th June	35th Anniversary Annual Symposium Bletchley Park, Milton Keynes
10 - 11th June	*IMFAIR09 - Institute of Metal Finishing RAF Museum, Cosford, Shropshire*
16 - 18th June	*National Electronics Week, Earls Court*
23rd June	12.30 ICT Council Meeting- Canal Museum
4th August	Joint ICT/MRC/EY Event at Rotherham
24th September	Southern Golf Day and PCB Dinner, Wiltshire Golf Club
6th October	17.00 Evening Seminar, - Norfolk Hotel, Arundel
3rd November	17.00 Evening Seminar, Devonport Hotel, Darlington

2010 Events

2nd Febuary	17.00 AGM - followed by Evening Seminar, Norfolk Hotel, Arundel
2nd March	17.00 Evening Seminar, Devonport Hotel, Darlington
12th April - 15th April	Annual Foundation Course , Loughborough University

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vol.2 no.3 July 2009

Editorial

ICT participates in European FP7 Project Proposal

The ICT has joined a consortium of potential project partners from across Europe in the preparation and submission of a proposal into the European Commission's FP7 call. The proposed project has a focus on solderable finishes and, in particular, is seeking to develop new approaches to the deposition and use of nickel-gold (ENIG), via the development of innovative process chemistries, and advanced testing methods for avoiding the problems that can influence the performance of these important solderable finishes. A key factor impacting the reliability of electronic assemblies is the quality of the solder joints and the nature of the circuit board solderable finish. ENIG has key advantages over other finishes and, despite its higher price, it is often the preferred choice in many advanced product applications. ENIG offers excellent solderability that is retained during prolonged storage and during exposure to multiple soldering cycles. ENIG finishes also have excellent planarity and this is crucial when assembling and soldering small fine-pitched surface mount components. However, while ENIG coatings have a good reputation for excellent solderability, there are a number of technical and economic factors which may cause problems. ENIG finished PCBs can suffer from problems specific to this particular coating technology. The most widely recognised is "black pad", which is attributed to corrosion of the nickel coating during the subsequent immersion gold deposition stage. Despite having been identified more than 10 years ago, the mechanisms that cause the effect (and the contributing factors) are still poorly understood. Moreover, no design rules, non-destructive testing methods, process optimisation/mitigation steps or viable alternatives currently exist. When ENIG-related problems occur, they usually affect an entire product design or batch.

This new project aims to help the European PCB fabrication and electronics assembly industries by developing new chemical deposition processes and methods for predicting, avoiding and detecting ENIG-related issues. The project also aims to strengthen the European electronics industry supply chain by helping ENIG users and by offering enhanced coating technologies. The project also aims to reduce the likelihood of ENIG-related problems occurring by improving the existing coating deposition technologies. Through plating development work, enhanced processes will also be developed that will enable thinner coatings to be used, thus reducing the cost of using ENIG while offering longer term reliability enhancements. Another key project goal is to develop methods for actually identifying potential problems related to the use of ENIG on PCBs during the production process. The project proposal is currently being reviewed by the European Commission's assessors and the ICT is expecting to receive the results of the assessment in August. If successful, the project will begin in 2010 and continue for three years, with the ICT playing a key role in the UK dissemination activities and the overall management of the project.

Professor Martin Goosey - ICT Deputy Chairman

Membership

New members voted into membership by the Council
23rd June 2009

Associate Member (A.Inst.C.T.)		**Member (M.Inst.C.T.)**	
Scott Hamilton	10130	Dr Tom Harvey	10148
Mike Gardiner	10131		
Gregor Wisneiwski	10132		
Witold Kandulski	10133		
Antonio Furlone	10134		
Darren Tait	10135		
Rob Austin	10136		
Richard Booth	10137		
Nick Norton	10138		
Stephen Brown	10139		
Paul Yeardley	10140		
Stephen McToal	10141		
James Mullan	10142		
Phil Dustin	10143		
Jane Razaq	10144		
Jake Cooke	10145		
Shefiu Zakariyah	10146		
Mark Capers	10147		

Corrections and Clarifications

It is the policy of the Journal to correct errors in its next issue. Please send corrections to : -
E-mail : bruce.rout@tiscali.co.uk

Len Pillinger F.Inst.C.T.
(The Institute of Circuit Technology-representative at REACh)

Does RoHS 2 have a costly sting in the tail?

Much of the industry breathed a sigh of relief when the proposed 'recast' (revised) RoHS Directive was published last December and only a relatively small number of new substance restrictions were announced. A list of forty-six became eight and finally five. This result was due to vigorous campaigning by trade and professional bodies, most notably IPC, to balance the enthusiastic and well-funded Green lobby.

As Gary Nevison of Farnell has noted in his 'Directive Decoder' blog; there is a definite sting in the tail for the electronics supply industry. The EU Commission are proposing to align RoHS with their 'New Approach' Directives. These are the ones that mandate CE marking of products, such as the EMC and Low Voltage Directives. You may consider this to be a responsibility for OEMs alone. However, OEMs have historically (and quite sensibly in many cases) devolved this responsibility to their supply chain and a whole CE marking industry has built-up around the needs of the supply chain. This industry needs to be funded and so adds cost to the electronics supply chain.

Consider parallels with the Low Voltage Directive (LVD):

In order to place an item of electrical equipment on the market within Europe, the producer (manufacturer, importer etc) must CE mark their products. This is now mostly self-declaration rather than third-party assessment. It is not therefore always necessary to have the product tested and / or certified by one of the many 'Notified Bodies' such as BEAB, BSI, UL or TÜV. These are organisations 'notified' to the EU Commission by Member States as being competent to pass judgement on products.

The producer will be declaring that his product meets the 'essential requirements' of the LVD, usually by reference to a Standard that has been 'harmonised' throughout Europe. A typical example is EN 60950-1 which covers the safety of Information Technology and Telecommunications Equipment. Such Standards detail or reference requirements for safety critical components and materials. Inevitably, a self-declaring producer (or their appointed test laboratory) will seek objective evidence that the isolation, self-healing, flammability and similar properties are as specified. This usually means third-party test reports or certification. Clearly, as a market entry qualification this is a cost to the component or material supplier.

To see the extent of this industry, consider that there are 158 Notified Bodies for the LVD alone in addition to countless test and certification laboratories around the world.

CE The PCB industry has been familiar with UL approval for many years as a 'must have' qualification, but the conversion of RoHS to a CE Directive may well increase the level of compliance resource required to satisfy customer demands.

What could this mean for RoHS 2?

There is already a 'RoHS Industry' populated by consultants, test laboratories, certification bodies and enforcement authorities. Mea maxima culpa – I was the proposer and helped to develop the BSI 'RoHS Trusted Kitemark' which has been awarded to a number of organisations across Europe. Similar schemes are being operated by BASEC, BABT, Bureau Veritas, SGS and UL.

A number of RoHS compliance schemes have been recognised by the UK RoHS Enforcement Body.

RoHS 2 is likely to give rise to similar OEM pressure given that they have the same legal hurdles to surmount. It is inevitable that this pressure will be passed down the supply chain and a significantly higher degree of RoHS compliance evidence will be expected.

So are there 'Harmonised Standards' that apply and with which suppliers will be expected to provide evidence of conformity?

One that has already been published after much debate is the test methods standard:

EN 62321 : 2009
Electrotechnical products - Determination of levels of six regulated substances (lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, polybrominated diphenyl ethers)

However, although RoHS 1 was published in 2002 and implemented in 2005, it was not until 2008 that the International Electrotechnical Commission (IEC) finally published this first 'RoHS Standard'. You will note that the new substances to be restricted by RoHS 2 are not covered. The analytical techniques called-up range from XRF to Gas Chromatography and are therefore beyond the budget of many organisations; hence the investment made by so many independent test laboratories.

Two further documents that are still in development are:

IEC 62474 Ed.1:
Material Declaration for Products of and for the Electrotechnical Industry

IEC 62476 TS Ed.1:
Guidance for evaluation of product with respect to substance use restrictions in electrical and electronic equipment

The title of the draft IEC 62474 makes it clear that the supply chain is being considered and not just the OEM / producer. IPC-1751 and IPC-1752 cover the same area. It is clear to see that RoHS 2 is likely to bring a much more formalised and structured approach to compliance with resultant increases in cost.

It gets worse! The UK legislation provides for those in the supply chain to be subject to enforcement and possible prosecution. The next two extracts are from the official UK Government guidance which can be downloaded from http://www.berr.gov.uk/files/file40576.pdf.

". The Regulations also provide for the 'liability of persons other than the principal offender', including a provision that where a company or other body corporate commits an offence, those concerned in its management and responsible (consciously or by negligence) for the commission of the offence, may also be prosecuted as individuals."

Light at the end of tunnel is provided by the potential for a defence of 'due diligence'

" The defence of 'due diligence' is available where a person can show he took all reasonable steps and exercised all due diligence to avoid committing an offence. This may include reference to an act or default of, or reliance on information given by, a third party, in which case it must be accompanied by such information identifying the third party, as is information in the possession of the defendant."

The UK RoHS enforcement authority is the National Measurements Office (NMO); formerly known as the National Weights and Measures Laboratory (NWML). I have found them to have realistic expectations of the industry coupled with a sympathetic approach where organisations have acted in good faith. Their expectation for 'all reasonable steps' is detailed at http://www.rohs.gov.uk/ along with other worthwhile guidance.

Likelihood and Timeframe

NMO are supporters of the principle of RoHS 2 being a CE marking Directive, and I understand that there is widespread support across Europe. It sounds like a 'done deal'.

Progress can be monitored by visiting http://www.berr.gov.uk/consultations/index.html. There has already been a public consultation on the European Commission's proposal and there will be a further chance to comment when the UK 'Statutory Instrument' has been drafted.

The European Parliament elections have slowed progress, but it is likely that RoHS 2 will be agreed in 2010 and implemented in 2012.

Len Pillinger F Inst CT
June 2009

Institute of Circuit Technology 35th Annual Symposium, June 2009

Bletchley Park, in Buckinghamshire UK, is the former stately home taken over by the British Government shortly before World War Two to be the secret base of the Government Code and Cypher School, which broke the reputedly unbreakable Enigma code and enabled British Intelligence to make sense of enemy communications: a historic and distinguished venue for the 35th Annual Symposium of the Institute of Circuit Technology.

ICT Technical Director **Bill Wilkie** Opening the Symposium, themed "Printed Electronics" welcomed faces old and new and reflected upon the continuing success of the Institute, and its steadily growing membership.

Keynote speaker **Dr Steve Jones** of **Printed Electronics Ltd** captured the attention and imagination of the audience with an enlightening overview of inkjet printed circuits and electronics, candidly subtitled "Trials, Tribulations and Some Success". In his introduction, describing electronics in a context of interconnecting components to form a functional device, he observed that people tended to talk not about the physics of how and why electronics worked, but about applications and functionality. His personal view was summed up "If I can't measure something, I know nothing about it – all I have is an opinion", and his objectives in Printed Electronics Ltd were to further understand the fundamentals of inks, the critical details of the generation of ink drops and their 1-millimetre journey between print-head and substrate, and their subsequent interactions with the substrate and with each other. He emphasised that whereas inkjet techniques have become firmly established in graphic arts, the electron was not as tolerant of image defects as the human eye, and a far higher order of precision was required in electronics applications. He discussed the relative merits of binary versus greyscale printing, with slow-motion video to illustrate drop behaviour and substrate interaction. On the subject of electro-active inks, he had studied an enormous number of proprietary silver nanoparticle formulations, some of which had given promising results when inkjetted, some not, and parameters such as curing profiles had been shown to have significant effects on functionality. Many applications had been explored, some typical, some unconventional – the programmable dinner plate, is it dishwasher-proof? Fitness for purpose, durability and reliability were key factors, rather than conformance with established standards. Potential scope for novel applications was limitless, and there was a need for those with a background in conventional interconnection techniques to adopt a different mind-set when considering printed electronics: "We have functionality, Jim – but not as we know it!"

Dr Neil Kirby recounted his many years of personal experiences in thick film technology with a review of the origins and historical development of printed electronics, from ceramic thick film applications in aerospace in the 1970s to the new printed electronics of the 21st century. A significant breakthrough had come with the development of low-temperature curing silver inks which could be used on polyester substrates, an early commercial example being the Sinclair ZX home computer in the early 1980s, featuring a membrane keyboard made using printed polymer thick film techniques. By the late 1990s, screen-printed interconnections, resistors and contacts could be found in mobile phones, electro-luminescent displays, remote controls for TV and video, calculators and disposable medical electronics such as electrocardiograph contact patches. Then came the sudden increase in interest in RFID in 1999, generated by proposals to replace barcodes for airport baggage tagging. Although RFID antennae could be mass-produced very cheaply by printing techniques, the cost of IC chips made the "one-penny tag" an unattainable goal. Printing of integrated circuits was a current mission for the printed electronics industry – not necessarily mission-impossible, but certainly mission-not-accomplished-yet. Dr Kirby discussed the evolution of materials, organic and inorganic, substrates and environmental issues, and surveyed current printed electronics applications in displays, lighting, smart packaging, sensors, batteries and photovoltaics, with many detailed examples. The future printed electronics industry had been estimated to be worth an annual £200 billion by 2020, most of which would be in new rather than replacement products, with materials development being the key issue. "Can do, can't do" questions were largely a matter of personal attitudes – whether people would be disablers rather than keep an open mind and be objective about the opportunities presented by emerging technologies.

Dave Wayness of **Dow Electronic Materials** focused on inkjet from a material supplier's perspective with a presentation entitled The Use of Inkjet Printing Technology for Fabricating Electronic Circuits, sub-titled The Promise and The Practical. The promise included elimination of photomasks, faster job turns, off-contact imaging for delicate substrates, image compensation and registration, higher yields and reduction in materials wastage. When it came to practical reality, inkjet fabrication of electronic devices was still very early in its maturing process and, echoing the comments of Steve Jones, although 300 dpi resolution was satisfactory for graphic arts it was far from adequate for electronics, which would require resolution of 750 to 5000 dpi for features to be continuous, uniform and functional. He discussed in detail the ways in which high-resolution images could be generated by multiple-pass and interlacing, taking as example a 75 micron line and space conductor geometry at 1250 dpi. Using an array of 15 heads, a 24" x 18" panel could be printed in 24 seconds. Dow had designed a hybrid UV

phase-change etch-resist ink, for use with heated print-heads – liquid at jetting temperature but solid at room temperature so that flow-out was minimal once it hit the substrate surface – which gave excellent image definition. There had been significant increase of interest in solder mask imaging, particularly on designs with solder-mask-defined pads where image placement accuracy was critical, and Dow's method of photo-tool elimination by inkjetting a UV-opaque negative image on to standard liquid photoimageable solder mask obviated all of the concerns regarding product qualification which had hindered the adoption of direct inkjet solder mask

Professor David Harrison's Cleaner Electronics Research Group had been working for many years at **Brunel University** on methods for producing circuit interconnects and passive components on various flexible substrates using offset lithography, a faster and higher resolution technique than screen printing. More recently, research had been directed at methods for producing voltaic cells by similar techniques, so that printed electronics devices could be powered by batteries produced in-situ. Leclanché cell chemistry, using zinc and manganese oxide with an ammonium chloride electrolyte, had been chosen as the basis of a feasibility study, and inks with properties suitable for offset litho printing had been developed to prove the concept. Changing from a zinc-particle to a zinc-flake system had improved performance, as had the use of a carbon intermediate layer and silver current-collectors. Batteries had been produced with capacities of 10 milliamp-hours, capable of delivering a peak current greater than 150 milliamps, although shelf-life remained a major limitation, 10 days being typical, and this was being addressed in ongoing work. Professor Harrison demonstrated as a working example a musical greetings card where both the interconnect and the battery had been produced by offset litho printing.

Frank Eirmbter of **SunTronic Electronic Materials** presented a broad survey of inks and chemicals for printed electronics. He explained the principles of various printing techniques – letterpress, gravure, flexo, pad, screen, offset and inkjet, and how the different processes required inks with different characteristics. The only printing process traditionally associated with printed circuit manufacture was flatbed screen printing, although rotary screen, rotogravure and flexography were now being applied to the production of hybrid devices and RFID tags. Offset lithography and inkjet printing were emerging as techniques for printed electronics. SunTronic were able to offer inks for all of these processes, and he listed many applications including antennae, membrane switches, capacitors, shielding , sensors, photovoltaics, RFID, displays, automotive, telecom, medical and diagnostic. Taking a membrane switch as an example, he described the manufacturing process and the specific products: graphics inks, silver conductive inks and flexible UV dielectric inks, used in fabricating the intermediate components. A second example he demonstrated was the construction of an RFID "smart label". RFID antennae could be printed directly onto cardboard boxes using a flexo-printed water-based silver ink. Other applications illustrated included flexible displays, printed resistors, transducers and sensors, and development would continue on functional inks for a whole range of new applications.

Stuart Hayton from **MuTracx** took the opportunity to describe an inkjet printing process specifically directed at defect-free imaging of inner layers, based on core competences developed over many years in MuTracx parent Océ group, with their own printhead technology, their own ink and a patented error-elimination feature.The Lunaris system was a drop-in replacement for traditional photolithographic and laser-direct-imaging processes, taking the work direct from base laminate to etch-resist image in a single step. Océ's extensive knowledge of drop flight and drop flow characteristics had indicated that a hot melt ink was most suitable for this application, and they had engineered a specific formulation compatible with their own design of heated print-head. The Lunaris machine incorporated 60 print heads, each of 260 nozzles capable of firing at 10 – 20 MHz. Although Océ's heads were claimed to be the most reliable in the world, statistically a failure rate of 1 in 1 billion droplets was expected, due to air entrapment in a print channel. A unique feature of Lunaris was the ability to predict such failure, and in operation only 1 in 3 print heads was in use at any instant, the system switching to an alternative row of heads every 20 seconds, with an additional row of heads always available as a standby, so that the one-in-a-billion failure was eliminated and a perfect image was guaranteed. The machine had a production capacity of 60 double-sided panels per hour, and was attracting keen interest in the market.

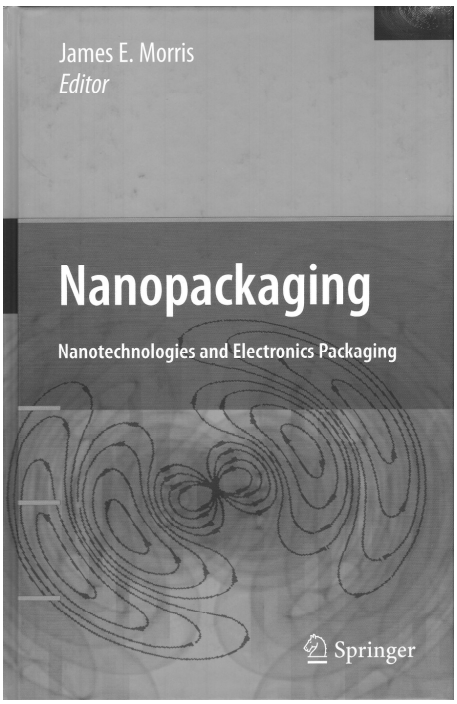
After Professor Martin Goosey, ICT Deputy Chairman, had wrapped up the proceedings and thanked the presenters, delegates were invited to take a tour of the Bletchley Park site, in the company of knowledgeable guides who explained its significance in the history of military intelligence. A highlight was the opportunity to see Colossus, the world's first semi-programmable electronic computer, meticulously rebuilt and fully operational, occupying a fair-sized room and with the cheerful glow of over 2500 thermionic valves. How things have changed...

Pete Starkey

ICT Council

June 2009

Book Review



Nanopackaging – Nanotechnologies and Electronics Packaging

Edited by James E Morris

Published by Springer
ISBN: 978-0-387-47325-3
e-ISBN: 978-0-387-47326-0

Nanotechnology is a field of applied science that is concerned with the production, manipulation and use of materials at or close to the atomic and molecular levels. A common feature of nanotechnology is that it deals with structures that have features with sizes of 100 nanometres or smaller, and it involves the development of materials and devices within that size range. In recent years there has been a surge of interest in nanotechnology as it has become clear that, by operating much closer to the molecular level, it is possible to achieve things that are not possible on a coarser scale. Materials can show markedly different properties and the ability to operate at the nanometre level opens up new possibilities for a wide range of devices and applications across many industrial sectors.

This is no more true than in the electronics industry where, ever since the birth of the semiconductor, there has been intense activity to make devices smaller and to build more functionality per unit area into silicon and other semiconductor materials. If one adheres to the definition that nanotechnology begins at the 100 nm mark, it can be said that the electronics industry entered the nano-world when semiconductor manufacturers moved to the so-called 93 nm node a few years ago. Today, commercial devices are available with 65 nm technology and the industry roadmaps show that feature sizes will continue to shrink until Moore's Law really does no longer hold.

It is not only at the silicon processing level that there is a drive to reduce device size. In order to be able to use these high density semiconductor devices, they also have to be interconnected and packaged and there is the same pressure to incorporate as much functionality into a given space as possible with packaging as there is with silicon. With its understanding of nanoscale operation and the inexorable drive to more miniaturisation, it is perhaps inevitable that the electronics industry is increasingly investigating the advantages that nanotechnology can bring to packaging and assembly, as well as to semiconductor processing. While there has been a huge amount of relatively disparate work undertaken on nanotechnology related to electronics, there is a real need for a consolidated work that covers many aspects of the potential for nanotechnology in electronics packaging and assembly. The new book 'Nanopackaging – Nanotechnologies and Electronics Packaging', which is edited by James E Morris and published by Springer, provides just such a work and it provides a welcome addition to the nanotechnology literature for those in both industry and academia who are working to develop the technologies that will enable us to benefit from continued innovation in future electronics.

A review of the contents pages of 'Nanopackaging – Nanotechnologies and Electronics Packaging' reveals that this is a very substantial work. With 23 chapters contributed by key nanotechnology experts from around the world, the book runs to an impressive 543 pages. Bearing in mind that many people working in electronics packaging will be new to the potential applications in which nanotechnology may be used and also relatively unaware of the benefits it may offer, the book sensibly begins with an introductory review chapter by the editor, James Morris. This opening chapter bridges the gap between nanotechnology and packaging by covering the potential scope for nanotechnology in this area and by providing over 100 references for further reading. There then follow three chapters that cover computer modelling in nanopackaging. The first of these, chapter 2, is provided by Professor Chris Bailey and colleagues from the University of Greenwich in London. This chapter takes a high level approach to nanoscale modelling for packaging that is complimented by examples of modelling for past, present and future applications. Chapters 3 and 4, by Fan and Yuen and van der Sluis et al respectively, both have their focus on molecular modelling techniques, especially for interfacial characterisation, with applications to carbon nanotube (CNT) thermal performance, moisture diffusion and thermal cycling and delamination failures.

The main part of the rest of the book then splits conveniently to cover nanoparticle and CNT related applications. In chapter 5 the editor, James Morris, contributes another chapter in which he introduces nanoparticle properties. Although relatively short, this chapter covers key aspects such as structure, electrical properties, melting point depression, sintering and mechanical and optical properties. The chapter is complimented by a comprehensive list of over 100 references. The fabrication of nanoparticles is mentioned in several chapters and Chapter 6 by Hayashi et al, concentrates on novel fabrication methods using an ecologically friendly sonochemical method.

The next three chapters cover the use of nanomaterials in passive device applications. There is a real need to enhance the dielectric, resistive, magnetic and related properties of materials used in passive devices, especially as they are increasingly being integrated into substrates as embedded components. Chapter 7, by Lu and Wong, covers the opportunities and challenges for nanoparticle high k dielectric composites. Metallic and dielectric filled composites have been of great interest in the electronics industry for many years and this chapter details the potential use of metallic and ferroelectric nanoparticulate fillers in both ceramic and polymeric matrices. Chapter 8 is by Wu and Morris and this chapter addresses nanostructured resistive materials. There is also an increasing demand for inductors and related components, especially in military, communications, automotive and portable electronics applications and chapter 9 by Jha et al covers the design, fabrication and packaging of nanogranular magnetic core inductors. It also gives a comprehensive review of inductor research and recent advances in the nanomaterials that are used in such high performance inductive cores.

The following three chapters have a focus on nanoparticles in conducting materials applications. Conducting and non-conducting adhesives find extensive use in electronics assembly and chapter 10 by Lu et al covers the nanoscale engineering of isotropically conductive adhesives. The chapter gives information on both nanoparticle additives and enhancements by surface treatments, as well as techniques such as low temperature nanosintering.

Once devices have been assembled and packaged they are then mounted onto the next level of interconnect and this is typically a multilayer printed circuit board. With the relentless drive to higher I/O counts and smaller package dimensions, the PCB industry has also had to respond by providing much higher interconnection densities in order to be able to integrate increasing numbers of devices on a diminishing size of substrate. These demands have led to the increasing use of sequential build up technologies and the incorporation of microvias in circuit board designs. There are numerous approaches to providing these conductive pathways but, as feature sizes get smaller, the challenges continue to increase. Chapter 11 is by Das and Egitto and it covers the use of nanoparticle based conductive adhesives in microvia applications. The chapter shows how nanoparticles and nanoparticle based adhesives are attractive for use in microvia fill applications. High aspect ratio small diameter holes can be successfully filled and the nanoparticle based materials exhibit sintering at lower temperatures, resulting in higher electrical conductivity. The materials are capable of giving high performance z-axis interconnects which can be made to meet or exceed JEDEC level requirements. Chapter 12 completes this group of three focused chapters and is by Felba and Schafer. It also discusses aspects of nanomaterials technology related to PCB interconnect applications and describes progress on printable solutions and the laser sintering of nano-silver based materials.

The use of nanomaterials in soldering applications has been under investigation for a while, especially in view of the largely legislation driven migration to lead-free assembly. There has been much work undertaken to study and enhance the reliability performance of lead-free solders and the incorporation of nanoscale materials into alloys has been one such investigated approach. In chapter 13 Amagai covers the addition of various nanoscale additives to tin-silver lead-free alloys. The addition of cobalt, nickel and platinum nanoparticles was found to have a significant impact in limiting intermetallic compound growth and thus the occurrence of mechanical failures by brittle fracture.

Chapter 14 is the final chapter of the book that covers nanoparticles and in it Lall et al detail the use of ceramic nanoparticle additives in underfill materials. A key issue with underfill materials is their relatively high thermal expansion coefficients compared to materials with which they are in contact. The addition of ceramic nanoparticles is reported to reduce the thermal expansion coefficient.

Carbon nanotubes are just one type of nanoparticle but their novel and interesting properties has meant that they have been a key area of nanotechnology research. The book therefore not surprisingly has a significant amount of space dedicated to CNTs and their use in the area of electronics assembly and packaging. In fact chapters 15 to 20 cover various aspects of CNTs and the first two (chapters 15 and 16) are from the same research group. In Chapter 15, Yadav et al cover the various techniques that are used to fabricate CNTs and chapter 16 then continues with a review by Kunduru et al of the basic properties of CNTs, their characterisation methods and potential uses. In chapter 17 Liu and Wang discuss the use of CNTs for the thermal management of microsystems, while chapter 18 by Cheng et al details the use of multiwalled CNTs in the electromagnetic shielding of transceiver packaging. There is a return to the subject of soldering in Chapter 19, where Kumar et al give information on the properties of conventional tin-lead and lead-free SAC alloy solders that have been reinforced with single wall carbon nanotubes. The chapter reports the results of studies into the impact that the CNTs have on the microstructural, mechanical, electrical, wetting and thermal properties of these composite solders. Interestingly, it was found that the addition of the CNTs reduced the thermal expansion coefficient of the solders as well as their melting points. The addition of nanotubes also significantly improved the creep rupture life of both leaded and lead-free composite alloys.

Chapter 20 is the final chapter covering carbon nanotubes and it is provided by Fielder et al. This chapter is titled 'nanowires for electronics packaging' and it covers a wide range of related subject

material including fabrication, materials and structures, as well as the interaction of nanowires with electromagnetic fields. There is also a discussion of future prospects and the authors provide well over 200 references. In chapter 21 Ma et al introduce a novel stress-engineered cantilever technique for forming free-standing interconnect wires or springs which is based on standard IC fabrication techniques. In addition to giving a detailed description of the fabrication processes for these molybdenum–chrome alloys, various applications are described including their use in non-soldered underfilled packages and sensing applications.

The penultimate chapter is by Mallik et al and it discusses the ever decreasing shrinkage of microelectronics features. This 22 chapter of the book has the title of 'flip chip packaging for nanoscale silicon logic devices: challenges and opportunities' and it is devoted to the shrinking CMOS issue. Starting with historical data, the chapter then provides an analysis of the nanometre CMOS challenges along with giving some insights into the future. Finally, chapter 23 by Zhang brings this tour de force to a well rounded conclusion with a top down overview of future industry directions as microelectronics moves firmly into the realm of nanoelectronics.

To summarise then, this is an impressive work that provides a substantial and relatively in depth coverage of a wide range of electronics packaging and assembly related applications for nanotechnology. Each chapter concludes with a list of references that can be used by the reader to further investigate a particular subject and the book is well produced with good quality figures and illustrations. The editor and publishers are therefore to be congratulated on bringing together in one place such a useful body of information relating to nanotechnology in electronics assembly and packaging. With a total of over 60 contributing authors and 23 chapters, this is clearly a very significant work and I am pleased to be able to conclude this review by rating 'Nanopackaging – Nanotechnologies and Electronics Packaging' as 'highly recommended'.

Martin Goosey
April 2009

EIPC Summer Conference 2009

June 18/19, 2009, Hotel Eggerwirt
St Michael im Lungau, Austria

The EIPC's 2009 summer conference was held in the picturesque Austrian town of St Michael im Lungau and it spanned two days, with a programme of 24 presentations, and a visit to the nearby IMPEX PCB drilling factory. This short report gives an overview of the conference and examples of the papers from each of the sessions.

The conference was opened by the EIPC's Chairman, **Rex Rossario** of **Graphic plc,** who gave an overview of the conference programme. Rex also stated that the key subject of the day was 'technology transfer' and he emphasised how this approach should be of use to the PCB manufacturing industry.

Dr Konrad Wundt of the EIPC then introduced **Walt Custer** of **Custer Consulting.** Walt gave another of his extremely detailed presentations on the current business outlook for the global electronics industry. He began by discussing the recession and stating that the industry had either bottomed out or was believed to be close to doing so. The UK had seen a negative 12.3% growth over the last year, with Europe, overall, being over 20% down.

However, there were a number of indices showing that the worst had probably been passed and the G8's finance ministers were now preparing for global growth.

Walt then went on to show inventory levels across the electronics industry and inventory relative to sales was now increasing.

The electronics industry had also been hit by the large drop in automobile manufacture. Interestingly, there had been a large growth in the production of'Netbook' computers, although they were typically low in price, so the benefits for manufacturers were not large.

Europe was estimated to now have around 240 PCB fabricators, with the largest producing country being Germany, which had 38% of European production. AT&S was the largest European board producer in 2008.

The conference then moved on to a series of themed sessions and the first of these, was entitled 'Business models for PCB success in Europe'.

The first paper was given by **Giacomo Angeloni of Somacis** in **Italy** and this was on strategies for survival. The survival strategy adopted by Somacis had involved partnering with Graphic and the establishment of some production in China via a new plant called DSG in Dongguan City.

In Europe, Somacis was the second most profitable PCB manufacturer and a new plant had also recently been set up in Italy with some funding support from the European Commission.

Michael Weinhold of the **EIPC** then gave a presentation on 'How to get business back from China'. Michael began by showing some of the recent good news that had been reported by the PCB industry.

However, European PCB production had continued to fall by value and, for 2008, it was less than half of the 2000 figure. Michael discussed the effect of exchange rates between China and Europe, which was now making Chinese PCBs more expensive.

Europe would always retain certain types of circuit board production such as high-end military and medical boards, as well as fast turnaround, special technology boards and development work.

The reasons influencing the choices between sourcing boards from Europe and China included quality, cost, technology, delivery time and after-sales service/design support.

The presentation concluded with a discussion of the opportunities available from the use of new technologies such as embedded capacitors.

The second session of the conference was on 'Advances in Materials'. The first presentation was given by **Thomas Michels of TMT Trading GmbH** and was titled 'The challenge of using no-flow prepreg versus bonding sheets in rigid flex applications'. He began by asking why the industry still used bonding sheets; and said it was largely because it had always done so.

The history of bonding sheets was then discussed and, in the past, these had originally only been available from Dupont as acrylic sheets. However, epoxy resin based products had also been produced to counter price and chemical resistance constraints of acrylic bonding sheets.

No-flow prepregs were also developed to meet the increasingly demanding technical requirements which included a need for higher Tg materials, the main driver being the automotive industry. Data was shown for no-flow prepreg that had been built into a 14-layer board and exposed to thermal cycling.

The IPC test method, IPC 2.3.17.2, was used to ensure flow measurements were meaningful. Properties of bonding sheets and no-flow prepreg were then compared and contrasted. The no-flow prepreg generally had a lower flow, better dielectric strength and enhanced through hole reliability. In summary, it was concluded that using no-flow prepreg gave the opportunity to produce more cost effective boards than with the use of bonding sheets.

The final presentation of the session was given by **Thomas Apeldorn** of the **University of Bayreuth** and was called 'Innovative substrates for PCBs based on thermoplastic polymers'.

Thomas began by explaining why thermoplastic substrates were used in some applications. Key positive points were said to include low dissipation factors, lower costs compared to conventional high frequency substrates and high operational temperatures.

Methods of fabricating thermoplastic PCB substrates were compared and contrasted with conventional fabrication routes and it was shown that it was possible to remove one or two processing steps.

The latest thermoplastic substrates could be inherently flame retarded and had the ability to be thermally shaped. They could also be recycled.

Techniques such as foaming, as well as blending and the incorporation of specific fillers had been investigated in order to tailor the substrate properties. The properties of these thermoplastic substrates were compared with those of standard substrate materials.

The so-called HTT foamed high temperature thermoplastic substrate manufacturing process was then described and this involved gas injection. The dielectric constant and dissipation factors were shown.

A material with an isotropic thermal expansion coefficient had also been developed. This had a CTE of 50 ppm/K and offered a two-step lamination process. For the so called LUVO and HT board types, the dielectric constant was low (~4.0) and remained almost level out to frequencies of ~1.2 GHz. These materials could also be shaped and further development work was needed before serious production could begin.

The first afternoon session was on 'advanced enabling technologies' and the opening presentation was given by **Martin Goosey** of the **Innovative Electronics Manufacturing Research Centre (IeMRC)** based at Loughborough in the UK.

Martin gave an introduction to the IeMRC and what it was seeking to achieve. He then went on to give an introductory overview of three of the IeMRC's projects that were related to printed circuit board and interconnect applications.These examples included the IeMRC's flagship project to integrate optical wave-guides into conventional PCBs.

He also outlined the printed electronics work being undertaken by Brunel University which, in addition to the

printing of conductors, had also moved on to the deposition of components, batteries and displays.

The third example highlighted work being undertaken at Coventry University to develop ultrasonically assisted methods for texturing materials used in electronics assembly e.g. PCB laminates.

By using enhanced ultrasonic techniques it was possible to texture materials at room temperature, using much less aggressive chemicals than those conventionally used.

The second presentation was given by **Markus Leitgeb** of **AT&S** and his presentation was called '2.5D technology platform – a novel approach to rigid flex and structural applications'.

He began by describing the future roadmap and the need to route two lines between the pads of a 400 micron pitch ball grid array followed by the need to provide one track between a 300 micron pitch BGA's pads.

The basic principle of the 2.5D technology platform was described and this used a standard structured core which was then screen printed with a release layer that enabled subsequent separation and removal of part of the processed board. An advantage of this cavity formation technique was that it enabled the use of standard base materials, gave much better accuracy in depth control, and no cutting process was needed. Boards were rigid and flat until the end of the process line.

Examples of test boards with components mounted in the board cavities were shown and these had been subjected to testing that had demonstrated their excellent reliability.

An HDI advanced rigid-flex PCB concept using a combination of polyimide and FR4 was also described.

Markus showed the cost reductions that were possible with the 2.5D technology and, in the example, given a saving of 15% had been achieved.

The final session of day one was on 'quality assurance and environmental issues' and it was moderated by **Michael Weinhold.**

The first presentation was by **Bill Birch** of **PWB Interconnect Solutions Inc**. and was on 'reliability testing for microvias in printed wiring boards'.

Bill began by reviewing industry trends and referred to the impact the RoHS Directive was having in increasing the levels of stress on interconnects and thus reliability. Higher lead-free soldering temperatures were leading to increased substrate damage, often inside the board where it was not immediately visible. New techniques were thus needed to find these impacts, for example, on stacked vias. The method Bill described was known as Interconnect Stress Testing (IST) and it utilised test coupons that contained heating and sensing circuits. The coupons were heated while the resistance was measured.

Bill also discussed various types of microvia based structures, such as stacked and staggered microvias, as well as the influence of microvia shape on subsequent reliability.

Coupon designs for the IST were also detailed along with the physics of microvia failure.

The next presentation was called 'An energy efficient final finish for PCBs' and it was given by **Melanie Rischka** of **Ormecon/Enthone.**

Melanie began by showing an example of an 'organic metal' molecule which was basically a conducting polymer that behaved like a noble metal and was similar to silver. It was also a nanometal with a 10 nm particle size and acted as a catalyst. The organic nanometal also prevented oxidation of metals such as copper.

It was used in a revolutionary new surface finish of which 90% of the deposited layer was organic. The organic metal deposition process was short and operated at a relatively low temperature. An environmental impact assessment of the new process had also been made and, compared to conventional HASL, it had a much reduced impact. Compared to ENIG the new process offered a 95% energy saving along with reductions in water consumption.

Various other studies had also been conducted and the process had a number of confirmed benefits over conventional surface finishing processes e.g. its green-house potential was lower than for all other finishes, including OSP.

The first session on the second day of the conference had a focus on 'How to improve efficiency in drilling' and was chaired by **Giacomo Angeloni of Somacis.**

Uwe Lenz of Ernst Lenz Maschinenbau GmbH gave the first presentation on 'Efficiency in drilling' and he began by stating that, in Europe, most PCB production was typically now prototyping and relatively low volume. This meant that there was a need for more flexible drilling machines that could both drill and route. These also needed to have a controlled depth drilling capability and broken bit detection.

Examples of mechanically drilled blind vias were shown, both before and after plating and it was claimed that they had better reliability performance than laser drilled vias. Being able to produce microvias on the same drilling machine offered significant efficiency gains. The use of a special tapered tool for drilling microvoias was also described. Uwe then moved on to discuss drilling machines that were more suitable for high volume production and the efforts that had been made to speed up the drilling process. It was also important that the drilling machines had a short set up time.

The final session of the conference also had a focus on efficiency improvements in drilling and it began with a talk by **Stephen Kurz** of **Schmoll Maschinen GmbH** on 'Influences on drill hole accuracy/quality in PCBs'.

There were a number of variables that influenced the drilling process and it was only the creation of optimum conditions that ensured drilling quality was achieved. These variables and factors were then introduced and they included the type of machine, the hole, the tool, the drilling parameters, the operating environment and the material being drilled.

The first example discussed covered materials including the entry material which could cause alignment problems if the surface was scratched.

Heavy scratching and debris on the top side of the aluminium entry material led to poor accuracy and increased drill breakage. The back up board and stacking process also had an impact.

Stephen then discussed the optimum drilling speed for specific materials and hole sizes e.g. the drilling speed for a 0.05 mm hole in FR4 needed to be 950 krpm.

Preventative maintenance could help maintain drilling efficiency and machines should be kept clean and properly serviced.

The pressure foot was also a potential cause of poor accuracy and a high vacuum force could lift the entry material leading to contamination, mis-registration and drill breakage.

The formal conference sessions concluded at lunchtime on the second day and after lunch the delegates were able to take part in a visit to the IMPEX Leiterplatten GmbH factory, which was also located in the town of St Michael.

In summary, this was a very successful and highly interesting conference that offered the delegates a wide range of up to date and useful technical and business information. It also provided an excellent networking opportunity for the delegates.

For more details of the conference programme or copies of the proceedings contact the EIPC via www.eipc.org.

Martin Goosey, 19 June 2009

SURFENERGY - a new European project to help the PCB and Surface Finishing Sectors

A new project supported by Intelligent Energy Europe called SURFENERGY has recently commenced with the intention of helping the European PCB and surface finishing sectors to reduce their energy consumption.

The title SURFENERGY is an abbreviation derived from the full project title 'Advanced Tools for SURFace Finishing Processes to Optimise ENERGY Efficiency', which gives a good summary of the project's overall objectives.

The SURFENERGY project is supporting the introduction of energy efficiency measures by Small and Medium Enterprises sized (SMEs) in the Printed Circuit Board and Surface Finishing manufacturing industry sectors and includes partners from the UK, Spain, France and Holland.

The aim of the project is to increase the awareness of manufacturing companies in these sectors to the introduction of energy management systems and the subsequent potential benefits that could result. The project outputs will provide options for energy efficiency solutions, based on a detailed analysis and understanding of the generic production processes currently in use by these sectors.

SURFENERGY is also addressing non-technological barriers to the introduction of energy efficiency measures through the main project actions which are as follows: development of an interactive software toolkit; process benchmarking; intelligence gathering on emerging technologies and integration with environmental assessment.

The project team plans to rigorously evaluate this toolkit via SME end-user applications testing during the second half of the project. The results of the project will be supplied to European companies via a targeted dissemination programme that will utilise industry trade associations and other routes that will increase awareness directly within industrial manufacturing SMEs. The strategic aims will support European policy objectives on energy efficiency and increasing competitiveness.

The expected results and outputs from the SURFENERGY project can be summarised as follows;

- An interactive software toolkit, based on technological analysis of generic processes, to facilitate options for energy efficiency solutions. The great majority of companies in the targeted industry sectors are SMEs and the project will therefore essentially address the non-technological barriers to the introduction of energy efficiency solutions to this type of organisation, within the context of the specific types of technology used in production processes.

- An energy efficiency benchmarking component of the toolkit will be developed and applied to the collection, analysis and reporting of data for generic processes currently in industrial use. Existing benchmarking approaches will be developed and tailored to the needs of the target audience and will be focussed on process-specific requirements. This approach will enable industrial manufacturers to compare their performance with industry standards and will act as an important stimulus for the implementation of energy monitoring and management.

- Intelligence gathering on new, emerging technologies and market drivers will be carried out. SMEs in the target groups often do not have sufficient resources to keep up to date with new technological developments that may have a strong impact on their future operations. Therefore, an important aim of the project is to inform the target audience about the energy efficiency implications of emerging technologies and the market/economic/societal drivers that may have an impact on their operations in the short to medium term.

- In addition to achieving excellence in industrial energy efficiency, all processes must be sustainable with a low environmental impact. In order to establish the environmental issues related to materials flow, including emissions to air and water, water usage etc., a simplified/streamlined Life Cycle Analysis approach will be applied to complement the detailed energy flow assessment.

- Targeted dissemination through the relevant trade associations and other routes will be used to increase awareness in the manufacturing sectors with high levels of 'market penetration'. These are traditional, SME-intensive industries, which are closely related technologically in that they operate many very similar industrial processes with overlapping issues in respect of the need to reduce energy consumption.

At the time of writing, the project has only recently started. However a technical assessment of the energy saving possibilities in the Printed Circuit Board and Surface Finishing sectors has been completed.

A comprehensive list of manufacturing processes has been compiled and savings

grouped into generic categories including: process improvement; retrofitting of more efficient equipment; waste reduction in existing processes; new processes and research developments. A project website has been established :-

www.surfenergy.eu or

surfenergy@ctechinnovation.com

for more details of the SURFENERGY project.

SURFENERGY is being supported by co-funding from the European Commission programme Intelligent Energy Europe.

Martin Goosey, 12th June 2009

One day - Training Workshops

PCB Design, Quality and Failure Analysis Workshops presented by Bob Willis

Three workshops enabling design and assembly engineers, PCB and assembly service buyers to understand how to assess and maintain printed board quality will be held at the laboratories of ITRI Innovation in St Albans, Hertfordshire and on site at Merlin Circuit Technology. Each workshop will combine both theoretical and practical sessions, and will be led by Bob Willis and assisted during the laboratory based practical session by the ITRI Laboratory Manager, Dr. Wayne Lam and Dennis Price of Merlin Circuit Technology. Workshops will be held in October and November: ICT Member are entitled to a 10% discount on booking any one of the workshops.

PCB Design for Manufacture & Assembly Workshop
15th October 2009 at Merlin Circuit Technology, Chester

"Having worked with Dennis Price since the early 90s I know his in-depth knowledge of the PCB industry and his practical experience and so running a workshop at Merlin will be ideal for delegates needing practical experience on design and manufacturing issues in today's ever challenging environment" commented Bob on the workshop announcements.

PCB Inspection & Quality Assessment – Practical Solutions
Tuesday 3rd November at ITRI in St Albans, Hertfordshire

Step by Step Electronics Failure Analysis
Wednesday 4th November at ITRI in St Albans, Hertfordshire

Further information on each workshop can be found at: www.ASKbobwillis.com/faworkshops.pdf

By sourcing PCBs from overseas or through distributors it can sometimes be difficult to assess the quality of incoming substrates. The switch to using lead-free assembly processes has highlighted issues of poor quality design and poorly fabricated circuits; thereby the need to understand available test methods is ever more important. By holding these events at the ITRI Laboratory delegates can witness the various techniques available for the verification of acceptable quality using a range of specialised techniques, which are not always available in their own facilities.

To book your place please visit: www.ASKbobwillis.com/faworkshops.pdf
Alternatively call Bob Willis (44) 01245 351502

Bob Willis

Group Members of The Institute of Circuit Technology July 2009

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Atotech UK Ltd.	William Street, West Bromwich. B70 0BE	01210 067 777 www.atotech.de
CCE Europe	Wharton Ind. Est., Nat Lane, Winsford	01606 861 155 www.ccee.co.uk
Electra Polymers Ltd.	Roughway Mill, Dunks Green, Tonbridge TN11 9SG	01732 811 118 www.electrapolymers.com
Faraday Printed Circuits Ltd	15-16 Faraday Close, Pattinson North Ind. Est., Washington. NE38 8QJ	01914 150 567 www.faraday-circuits.co.uk
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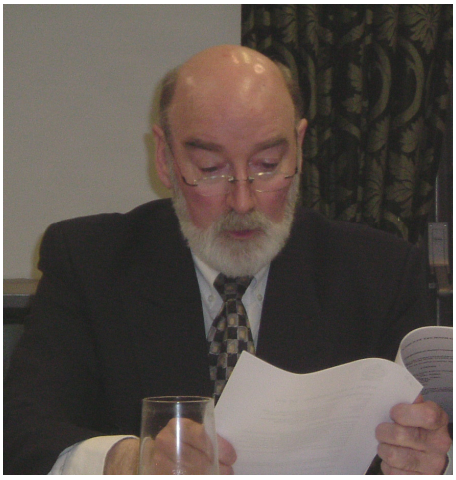
Tru-Lon Printed Circuits (Royston) Ltd.	Newark Close, York Way Ind. Est., Royston SG8 5HL	01763 248 922 www.trulon.co.uk



The Membership Secretary's notes June 2009

We recently held our 35th Annual Symposium at Bletchley Park and reflected on the world of 35 Years ago in 1974. At our events, delegates talked about strange chemistries such as pyrophosphate copper and that young upstart – high-build copper had been with us for a few years, but was not that reliable. We did have dry film, which was gradually replacing screen print, but it was mainly solvent processable using 1,1,1, Trichloroethane as a developer! Shops were springing up all over the place, crying out for better, more reliable products and closed shops, like IBM, Burroughs, ICL, Philips, Rank Xerox, Ferranti and GEC Marconi were not only manufacturing boards, but also conducting their own research.

It was into this maelstrom of technological advances that the ICT was born, in what was a burgeoning new industry. Part of our Charter, called upon us to supply venues, meeting rooms for the exchange of information and we continue doing that today.

Edited by Bruce Routledge on behalf of the
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