

# Journal of the Institute of Circuit Technology

Vol.5 no.1 Winter 2012 Issue

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## 2011 Events

- 1st November **17.00 ICT Evening Seminar.**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)  
 "Supporting Industry Needs"  
 Devonport Hotel, **Darlington**  
<http://www.devonporthotel.com>  
 supported by LAMAR GROUP
- 9th November - 12th Electronic Circuits World Convention  
 11th November Taipei Nangang Exhibition Centre, **Taiwan**  
<http://www.service@ecwc12.org>

## 2012 Events

- 2nd February - EIPC Winter Conference,  
 3rd February Prague, Czech Republic
- 8th February 17.00 Registration  
**17.30 ICT Evening Seminar.**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)  
**Norfolk Arms Hotel, Arundel.**  
<http://www.norfolkarmshotel.com/>  
 supported by CCI Eurolam
- 26th March - **ICT/NUKCG Annual Foundation Course**  
 29th March at **Loughborough University**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)
- April National Electronics Week (NEW)  
 Birmingham

Welcome to the first issue of Volume 5 of the ICT's Journal. This issue has a wide range of technical articles and related information that should be of great interest to all members. For example, the ICT is leading a multi-partner European project called **ASPIS** that intends to develop new, more reliable solderable finishes based on nickel and gold. The problems associated with these types of finishes have been well documented over a number of years, but there is still not a full understanding of the basic failure mechanisms around such problems as the dreaded 'black pad'.

The project has recently completed its first year of activity and we thought that it would be appropriate to provide a summary of the work undertaken and the progress made to date. To that end, I have written an article for this issue called, 'Advanced Surface Protection for Improved Reliability PCB Systems (ASPIS) – 12 months of progress' which gives an overview of what we have done and what has been achieved in the project. I hope you find it of interest and I would be happy to receive your feedback, suggestions and comments.

I am also pleased that we have been able to include a really novel paper describing research undertaken by some of my colleagues at Loughborough University. This paper details work on a multi-electrode array biochip with excimer laser-produced micro-well features. Apart from reporting details of some potentially very important and valuable work, this paper also serves to show how widely the formation of circuitry is an important component in many new types of electronic devices. Again, I trust that you will find the details of this fascinating work of interest.

In addition to these two papers, we have information about another new EC-funded multi-partner project that involves members of the ICT. This project is called **Susonence** and it is developing advanced sonochemical processes to reduce chemical usage and decrease waste in the PCB and metal finishing industries. This project has only recently commenced, but we will bring you more details of progress in future issues.

As usual, our roving reporter, **Pete Starkey**, has provided us with reviews of a couple of recent highly successful events, namely the **ICT's November evening seminar** in Darlington and a webinar organised by Bob Willis called '**The Good, the Bad and the Ugly**' and which addressed PCB Nickel-Gold Surface Failures.

We are always happy to receive inputs for the journal in the form of papers, articles, reviews and news about your company etc, so please feel free to submit your contributions for publication. Finally, may I wish you all a happy and prosperous 2012 and I look forward to seeing you at one of the numerous events that the Institute has arranged during the coming year.

Martin Goosey  
*ICT Chairman*

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**Council** Martin Goosey (*Chairman*), Andy Cobley (*Deputy Chairman*), John Walker (*Secretary*), Chris Wall (*Treasurer*),  
**Members** William Wilkie (*Membership Secretary & Events*), Bruce Routledge (*the Journal*), Richard Wood-Roe (*Web Site*),  
**2011/2** Lawson Lightfoot, Tom Parker, Steve Payne, Peter Starkey, Francesca Stern, Bob Willis.

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### Membership

New members notified by the Membership Secretary

| Member (M.Inst.C.T.) |                   | Fellow (F.Inst.C.T.) |                 |       |             |
|----------------------|-------------------|----------------------|-----------------|-------|-------------|
| 10208                | Martin Black      | 10220                | Andre Dalby     | 10214 | John Ennis  |
| 10209                | Graham Barbour    | 10221                | David Douglas   | 10218 | Neil Martin |
| 10210                | Bill Pegram       | 10222                | Brian Morgan    |       |             |
| 10211                | Adam Tree         | 10223                | Tony Cornish    |       |             |
| 10212                | Paul Rushforth    | 10224                | Rozanna Griffin |       |             |
| 10213                | Derek Reeves      | 10225                | Brian Bishop    |       |             |
| 10215                | Paul Kane         | 10226                | Steve Thornley  |       |             |
| 10216                | Michael Wellstead | 10227                | Keith Hole      |       |             |
| 10217                | John Cunningham   | 10228                | Jeremy Wakeford |       |             |
| 10219                | Edward Smith      | 10229                | Simon Beckett   |       |             |

### Corrections and Clarifications

*It is the policy of the Journal to correct errors in its next issue.*

*Please send corrections to :-*

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## Susonence – a new multi-partner project developing advanced sonochemical processes to reduce chemical usage and decrease waste in the PCB and



**Prof. Martin Goosey**  
*Chairman*

Institute of Circuit Technology

A new European multi-partner development project has recently commenced to introduce more efficient and cleaner production into the PCB and metal finishing industries.

The project will employ sonochemical processes that decrease hazardous chemical usage and minimise the amounts of waste generated. Energy consumption will also be reduced by the use of new processes that operate at lower temperatures for shorter times.

The three year project is known as Susonence, an abbreviation of Sustainable Ultrasonically Enhanced Chemical Processes, and it is being supported via the European Commission's CIP Eco-innovation scheme for 'First Application and Market Replication Projects'.

Susonence has seven partners from across Europe, including three UK-based organisations,

C-Tech Innovation Ltd,  
Env-Aqua Solutions Ltd  
Coalesce Solutions Ltd.

The other partners are  
Pragoboard s.r.o. Czech Republic,  
Protection des Metaux S.A.S. (Promet)  
International Project Management,  
Plating and Materials, France  
EIPC Services B.V., Netherlands.

Together, these organisations represent a broad cross section of the requisite industry supply chains and several of them have already worked together on other projects.

The key aims of the Susonence project are to implement ultrasonically enhanced surface modification processes for removing surface layers, etching, and texturing a variety of widely used substrates (metallic, polymer, ceramic) with greatly decreased chemical consumption that will enable a step-change in competitiveness within the surface finishing and printed circuit board manufacturing sectors, whilst significantly decreasing environmental impact.

Susonence is a first application project bridging the gap between research and the marketplace and will take an already demonstrated new technology, via the design and scale-up of the ultrasound treatment systems, towards successful, economically viable industrial processes for both of the PCB target sectors.

A major part of the project will be to optimise solution chemistries based on dilute water-based formulations specifically developed for each application, i.e. the aim is the replacement of existing corrosive and/or toxic chemical formulations, which often operate at high temperatures.

One target process will be the conventional high temperature permanganate-based desmear operation,

which uses both solvents and strong oxidising agents.

Another target process will be the chromic acid surface treatment stage used for texturing the surfaces of polymers such as ABS prior to metal plating.

This reduction in the use and concentration of hazardous chemicals will lead to more sustainable and environmentally friendly processes that will additionally offer significantly reduced waste treatment costs due to the use of less-hazardous chemicals.

The new ultrasonic technology will also offer decreased energy consumption via reductions in the operating temperatures of the target processes and the time taken to complete a specific chemical treatment stage.

The project will achieve these aims by the implementation of advanced sonochemical systems scaled up for industrial application, with four main areas of innovation :-

- The first is the realisation of the potential for achieving surface modification treatment of a wide range of substrates through the application of acoustic cavitation, while at the same time greatly reducing the chemical content of surface pickling and etching solutions.
- The second is a novel concept of formulating cleaning/etching/pre-treatment solutions specifically for use with ultrasound.
- Thirdly, this project will also optimise and incorporate an innovative and novel method of applying ultrasound for surface modification through the use of optimised ultrasonic frequencies and transducers.
- The fourth innovation is the design and scale-up of optimised surface treatment processing equipment integrating these novel ultrasonic probes/transducers and control systems whose design is tailored to specific substrate configurations.

The Susonence project aims to implement the first industrial scale plants incorporating the new ultrasonically enhanced process technology within the project partners' facilities in the metal finishing (Promet) and printed circuit board (Pragoboard) manufacturing sectors.

Key factors that will encourage the adoption and uptake of the developed technology are the increasing costs of raw materials, energy, and treatment of waste and ultimately the disposal of waste from site, which are all projected to continue to rise inexorably due to a combination of legislative demands in the instance of waste and escalating world demand, primarily from Eastern manufacturing areas.

As a result, there is clearly defined competitive need, and an opportunity, to achieve significant cost benefits in the reduction of direct manufacturing overheads in these strategically important sectors of European industry.

The major outputs from the project will be five industrial scale units matched to the needs of the targeted sector manufacturing plants. These plants will then be used to collect detailed field trial data that will enable the true performance benefits to be accurately determined and further iterative improvements to be made to the equipment and processes.

Based on the construction and operational data generated, other key objectives will be to undertake techno-economic modelling and a life cycle assessment to determine the overall environmental impact and benefits compared to traditional processes.

These benefits are expected to include: -

- reduced use of toxic/ hazardous chemicals
- waste minimisation/ diversion from landfill
- reduced energy consumption
- reduced water consumption

and the operation of each of the five pieces of equipment in true industrial manufacturing environment with a range of processes will enable them to be fully assessed and demonstrated.

The Susonence project is thus aiming to help the European PCB fabrication and metal finishing industries by

developing new processes that are more efficient than conventional processes through the use of advanced ultrasonic technology.

Subsequent uptake of the technology industry is expected to provide environmental, economic and societal sustainability benefits by virtue of the reductions in hazardous chemicals used and associated cost savings, cost benefits from reduced energy, waste treatment and waste generation/ disposal as a manufacturing overhead reduction and greater competitiveness for the targeted manufacturing sectors within Europe.

The new processes will also enable European companies in the PCB and metal finishing sectors, and their customers, to produce more competitive products via both increased process and assembly yields and to provide higher levels of quality in finished products.

Further information about the Susonence project is available from a dedicated website, [www.susonence.eu](http://www.susonence.eu), and there will also be a wide range of publications and dissemination activities throughout the life of the project.

**Martin Goosey**

September 2011





## A Multi-Electrode Array (MEA) Biochip with Excimer Laser - produced Micro-well Features.

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### Introduction

Rapid development of multi-electrode array (MEA) electrophysiological recording systems is occurring across both research and industrial settings. The use of MEA technologies is well-established in neurological research, however in recent years more interest has been focused upon the true bioscientific potential of these tools in numerous other cell-based research settings.

New questions relating to how best to optimise acquisition of data from differing cell sources and how to best extract meaning from those data are evolving.

Although there is interest from a diversity of bioscientific applications focus is especially strong in stem cell (SC) [1-3], and drug discovery and development applications [4-6].

Recent evidence of MEA system application in differing research domains and the consequent development of new components and full systems can be reviewed in previous Proceedings of the MEA Meeting, held bi-annually in Reutlingen, Germany [7-9].

An MEA system serves the purpose of detecting and recording the microvolt level electrical signalling that occurs through living cells or tissue.

The vast majority of studies conducted using MEA technology investigate electrogenic tissue types (i.e. neural and cardiac tissues) [6] but work exploiting other non-electrogenic cell types has also been conducted [10-13] monitoring slow ion fluctuations that differ greatly from the spikes and bursts of electrogenic cells.

MEA system-based experiments are limited in the volume of data that can be acquired. Limitations can be attributed to several causes such as the set-up and application being time intensive [14], the consequent data analysis is also timely and often complex [15], and there is a lack of standardisation across users of equivalent applications [16].

This lack of standardisation has resulted in numerous differences in approaches and protocols from one equivalent MEA user group to another. MEA systems are needed that allow experiments on much larger scales to be performed [17]. The result of which will be an increase in volumes of data generated, and this will in turn require more advanced data processing, that is ideally within a shorter period of time.

Standard commercially available MEA biochips typically consist of a small square glass substrate with 60 microelectrodes embedded at the centre. A cellular preparation is either placed or cultured over these microelectrodes. An underlying network of electronics work to amplify, filter and convert the microvolt analogue signals detected into digital data streams that can be manipulated by the user via a PC.

In the case of users that exploit MEA systems in the characterisation of cardio-active substances, it is essential

that the beating cardiomyocyte cell sources form a physical attachment to the MEA base substrate. This attachment must be over, or in very close proximity to, the microelectrodes (fig. 1); without it no signal will be detected. Due to the contracting nature of the cell source and the motion of transit when moving the biochip around a laboratory, it is common that the beating cluster attachments are formed in locations away from the initial seeded position

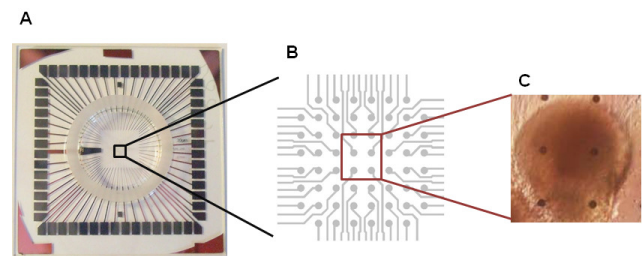


Fig. 1: A) A standard commercially available MEA biochip. B) The surface area of the biochip that is referred to as the workspace, where the microelectrode tips are embedded.

C) An attached stem cell-derived beating cluster of cardiomyocytes over microelectrodes.

As in-vitro recording using MEA systems continues to grow, it has been widely recognised that the development of the MEA biochip has relied heavily upon the timely progression of suitable fabrication techniques [18].

Generally, MEAs are designed on a planar surface using conventional microelectronics or micro-electro-mechanical system (MEMS) technology; this involves thin film deposition and various photolithography techniques [19].

Popular commercially available MEA biochips are typically manufactured using glass-based substrates; resulting in rigid and fragile samples. The microelectrodes manufactured at the centre of the base substrate are presently made from titanium nitride (TiN), platinum (Pt) or gold (Au). Configuration is traditionally in an 8x8 grid array, where one electrode has been removed at each corner of the array, resulting in a total of 60 microelectrodes in a standard MEA biochip.

The emergent standard geometry of the microelectrodes within the 8x8 arrangement is 30  $\mu\text{m}$  dia. spaced with a pitch of 200  $\mu\text{m}$ . Therefore, the total area of the base substrate that is exploited as the MEA

“workspace” is less than 2  $\text{mm}^2$ . The biochip’s upper surface is insulated on standard MEA biochips by spin coating or plasma enhanced chemical vapour deposition (PECVD) of a suitably biocompatible material. Only the microelectrode tips and interconnects skirting the periphery are left exposed to the environment. Commonly used insulation materials include silicon nitride and the

epoxy-based photoresist SU-8, which are known to be chemically resistant and relatively impermeable to environmental moisture and ions [19, 20].

The microwell feature that is being incorporated into the biochip design that is presented in this paper does not require application of such an insulator as the electrodes, conductive tracking and interconnect contact pads are manufactured on a base substrate that is covered by a thin layer of epoxy and polyester film; therefore insulating the circuitry from the liquid media required for cell culture.

This design change could potentially eliminate the current requirement to pre-treat the MEA workspace with a suitable attachment matrix prior to seeding the living cells thus saving users time and reducing costs.

## Enterprise Modelling

Enterprise modelling approaches have been made use of throughout this work to track and monitor the processes that are critical to the future feasibility of this design concept as a scalable product. A specific architecture has been used to construct models that allow developers to ensure important information is collected and presented appositely.

One architecture, Computer Integrated Manufacture Open System Architecture (CIMOSA), has been employed to construct these models to ensure comparability. This single architecture has been applied to modelling of all processes that impact upon this work. Modelling of MEA biochips in use and also modelling of how the Loughborough University biochip prototypes are manufactured has been conducted.

Timing inputs and resource consumption information derived from the models constructed provided the development team with relevant information pertaining to concept validation and also manufacturing scalability.

Enterprise modelling was used to track consumables use and labour inputs throughout the product innovation process, allowing costs of manufacture to be monitored as alterations to the manufacturing approach were made, leading to the prototype described.

The data was captured and reviewed interactively as workflow amendments were made, allowing developers to ensure that every aspect of the manufacturing process could be monitored and communicated as required.

## Material and Process Selection

The most commonly used polymers considered to meet this design preference were polyester, polyimide, liquid crystal structures and polydimethylsiloxane. Polyester and polyimide in film forms exhibit a combination of properties otherwise shown in a number of other polymer films either individually or in inferior combinations. Properties exhibited by these films include low stress, low moisture uptake, high modulus and good ductility. These properties are ideally suited to biotechnology applications. A commercially available example of a polymer film suited specifically to cell growth is Melinex® from DuPont, which is a polyester film that has been treated specifically to enhance cell attachment [21].

The Excimer laser is a laser variant that can facilitate formation of micrometer scaled structures that is frequently applied with these types of materials, where a high degree of design flexibility or complex patterning is required. The properties of the Excimer laser that make its use excellent in

such circumstances are its high resolution, good precision and high coupling efficiency [22]. The authors of this paper identified the potential to use Melinex® film in unison with an Excimer laser to produce enhanced MEA biochip features.

## The Manufacturing Workflow

Fig.2 depicts the manufacturing workflow and the proposed novel MEA biochip concept. One biochip that can reliably contain more than one beating cluster is desired. Microwell features are located over each electrode to limit the movement of the beating clusters during the attachment period. Firstly, standard FR4 substrate material was used with a 70 micron copper foil coating (Mega Electronics Ltd, UK). The copper was patterned using conventional photolithography and etching processes. Samples were then outsourced to an external company for Au coating (PMD Group, Coventry). The Au coating served to seal in the Cu, which is toxic to living cells, thus producing a cell-friendly contact surface on the 1 mm diameter electrodes. The Au coating was approximately 3-5 µm thick. The Au plated substrates were cleaned in 70% ethanol (30% water) using an ultrasonic bath to remove any dust or debris that may have resulted from the manufacturing processes and to sterilise them.

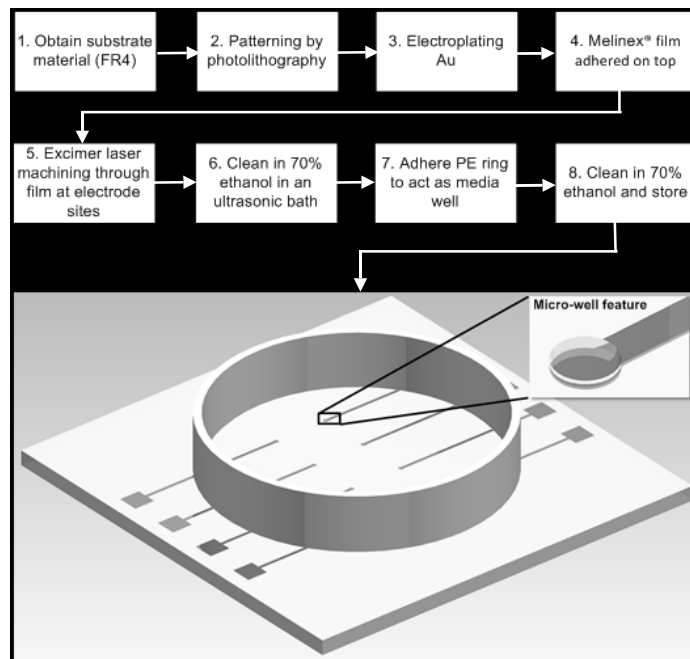


Fig.2: *Manufacturing workflow schematic and a CAD model of the intended prototype.*

A cut-to-size disc of Melinex® film was adhered on top of the electrode sites in the location of the future media well. An Exitech Excimer laser, consisting of a short-pulse laser source (KrF, wavelength 248 nm) and an Aerotech positioning system, was used to prepare microwell features directly over each electrode site with a diameter of 500 µm. The laser application was tested using alternative substrates, including standard glass and polyester coverslip material and the specialist Melinex film. All samples compared were of equivalent thickness. The Melinex film demonstrated the best compatibility with the laser process as the lowest number of pulse repetitions were required to reliably and consistently produce the microwell features.

On all prototype substrate samples Melinex® film was laser ablated until the underlying Au surface was exposed;

the depth of the microwells was therefore equal to the thickness of the Melinex® film, 190 µm.

Different size and shape microwells can be made by making various ablation masks, replacing the circular one used in this instance.

Microwell features have been incorporated into the design in attempts to ensure attachment occurs over an electrode site, therefore guaranteeing more than one signal that can be used in analysis – one signal per test repetition is currently the case.

Finally, samples were cleaned again in an ultrasonic bath prior to the addition of a polyester (PE) ring, made from a cut-to-length standard industrially available PE tube. The PE ring was adhered directly onto the Melinex® surface using a non-toxic silicon-based adhesive.

### Process Time

The process time required throughout the various manufacturing workflow stages was captured using the aforementioned, internationally standardised CIMOSA (computer integrated manufacturing open system architecture) enterprise modelling techniques[23]. Fig.3 and 4 present the stages of manufacture that differ most significantly from those used to produce commercial MEA biochips; production of the MEA base substrate and production of the microwell features. It has been of interest to monitor and quantify resource use and time in production so that scalability following initial proof-of-principle could be assessed. It is intended that these biochips will be significantly cheaper than commercial glass-based biochips.

(2) Cu Patterning by photolithography

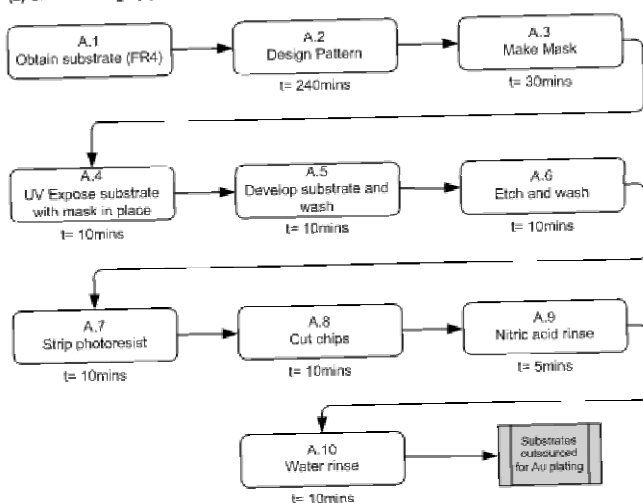


Fig. 3: A simplified CIMOSA (Computer Integrated Modelling Open System Architecture) activity model of the workflow developed to produce the base substrate and the associated labour times.

(5) Excimer laser

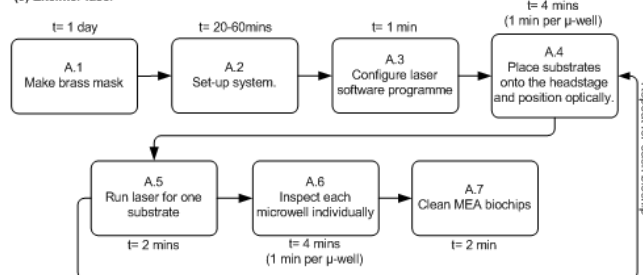


Figure 4: A simplified activity model of the workflow and associated labour time for creation of microwell features at electrode sites.

### Results

Biochip prototypes were inspected following manufacture and cleaning prior to approval for live trials.

The following results were generated during the combined assessment of the novel manufacturing approach and the resulting microwell integrated prototype MEA biochips. Assessment of materials biocompatibility and success in terms of the manufacturing combination with respect to in-use characteristics has been pursued.

The base substrate and microwell features were optically inspected for consistency and defects. A cross section micrograph was used to view the microwell feature in detail and assess geometry. Fig.5 reveals that the Excimer laser adequately removes the Melinex® film to expose the underlying gold surface.

Conductivity measurements using a Hewlett Packard 4284A LCR multimeter also showed that the machined surface had good conductivity, implying that no insulator film remained at the bottom of the microwell

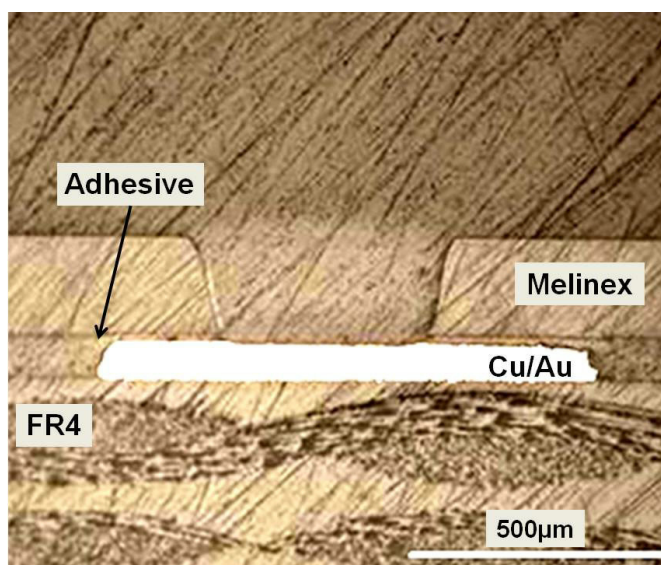


Fig. 5: A cross-sectional micrograph image of the microwell feature.

The alignment of the microwell feature over the underlying electrode was variable across prototype samples manufactured. This was due to the ‘by-hand’ alignment of the samples on the system’s headstage. This is a manufacturing parameter that can be more reliably controlled in future prototyping to allow a greater degree of freedom in the experimentation of microwell geometries.

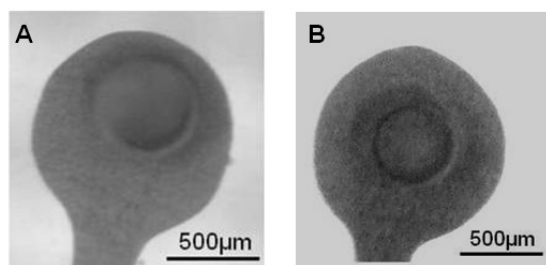


Fig.6: Optical micrographs of microwells under media conditions, demonstrating variation in position of microwells relative to the underlying electrode. A) Microwell containing a human Embryonic Stem Cell ( hESC)-derived cardiomyocyte cluster with Imprecise alignment. B) An empty microwell showing improved alignment.



Testing of this device was completed in small batches due to constraints on the number of beating clusters that could be acquired for this work.

Beating clusters seeded into the Loughborough manufactured biochip prototypes showed varying successes in terms of cell attachment.

Stem cell (SC) derived cardiomyocytes are still a comparatively new cell source, and as such are under constant attention in terms of improving beating cluster reliability of production and control over inherent variability.

Variations in attachment success is thought to be due to both the size and shape of the beating clusters, as well as due to movement to the incubator and from cellular contraction.

A beater successfully attached inside a micro-well can be seen in Figure 6A. From these observations, the suitability of the materials selected in manufacturing and the approaches used to realise the novel concept can be confirmed.

Responses from the end users were recorded, highlighting concerns specifically relating to the increased optical constraints of this design when compared to commercially available alternatives. Commercial chips are made on glass with electrode geometries that are smaller than the cellular sample. This allows users to visually confirm that their sample is both attached to the biochip surface and is still contracting prior to, and throughout, recording.

Quantitative information derived from the deep level CIMOSA modelling of the bioscientific processes (i.e. laboratory protocols) of MEA employment has also been completed.

The level of detail used has made it possible to estimate where time savings are probable during biochip use in the target application domain.

Data shown in Figure 7 indicates that the design changes implemented in this setting could save users approximately 8 hours of set-up and trial time. In this instance, 8 channels (and therefore beating clusters) will also be assessed in one test.

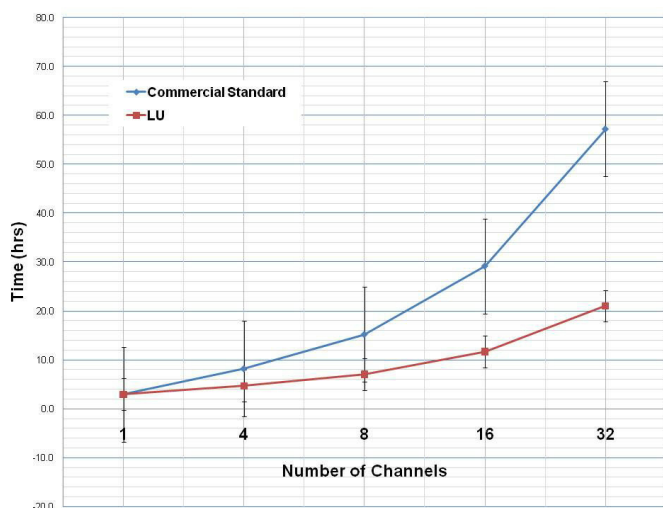


Fig. 7: *Projected labour saving for this design vs. commercially available standard, based on real-life timing data extracted and documented. LU = Loughborough University MEA biochip. Prototype biochips presented 8 electrode sites, providing an opportunity to capture the equivalent amount of data to 8 sequential trials performed using a standard commercially available biochip.*

The seeding of more beating clusters is required before results can be reported pertaining to the quality and reliability of the signal acquisition. A custom built headstage unit is under development to provide appropriate amplification and filtering required for signal utilisation.

It has also been identified that alterations to the current graphical user interface (GUI) to accommodate the design changes implemented would simplify the testing of these prototypes.

An image of the intended interface alteration has been generated (fig. 8) where 8 channels show 8 unique beating clusters available for testing in the same media well at the same time.

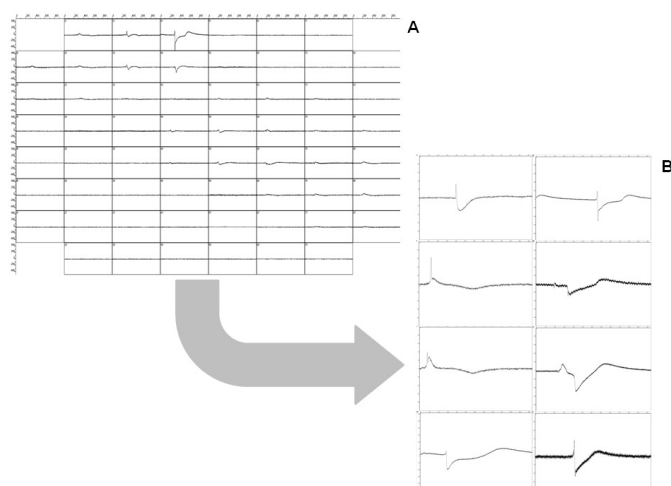


Fig. 8: *Required GUI alteration. (One file of data is output per test repetition.)*  
 A) *The current GUI display for standard commercial 60 microelectrode MEA biochips where one usable channel is present per data file.*  
 B) *The required output display to complement the design changes introduced by the Loughborough University MEA biochip where eight usable channels will be present in each file of data.*

## Conclusion

Biocompatibility of material choices and suitability of the manufacturing approach have been assured as a result of this preliminary work.

The manufacturing approach presented has allowed a new biochip design to be demonstrated that permits more recording sites per single media well. Consequently, less time is spent on day-to-day culture maintenance, there is an increased ease of initial cell positioning due to the microwell features, and chemical treatments (such as drug candidates) can be administered to all of the cells in a trial at exactly the same time without the requirement of an expensive perfusion system.

These advantages deliver increased convenience and consequential time and cost savings to user groups in this particular application.

Further attention is required with regard to the microwell dimensional optimization, optical inspection conveniences, and quality of the output signals. Further attention is also required in the development of a suitable user friendly graphical user interface (GUI).

## Acknowledgements

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The authors would like to give special thanks to PMD Group, Coventry, UK for their expertise and efforts in the gold electroplating process.

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## Introduction

There are increasing numbers of different solderable finishes in use and these include hot air solder levelling, organic solderability preservatives (OSPs) and nickel-gold (ENIG). However, for many years, the preferred choice of finish for high reliability, high performance electronics has been nickel-gold, because it offers benefits such as excellent solderability that is retained after storage and during the multiple soldering operations required with high value electronic equipment.

However, while ENIG coatings have excellent solderability, there are a number of technical and reliability factors that can sometimes cause problems for PCB fabricators and their customers. The most widely recognised of these is 'black pad', which is thought to be attributable to excessive corrosion of the nickel coating during the subsequent immersion gold deposition process.

Despite having been identified many years ago, the mechanisms that cause 'black pad' are still poorly understood. This paper outlines some of the progress made during the first year's work on the 'ASPIS' project which is developing new, more reliable nickel-gold materials and processes.

The three year project is being coordinated by the ICT and it is supported via the European Commission's 7th Framework Programme. Aspiss is a 'Research for SME Associations' project that has twelve partners from across Europe, including four key research organisations who are undertaking much of the research programme.

The ASPIS project has four discrete approaches and these are;

- 1) research into 'black pad' formation methods,
- 2) investigation of improved traditional aqueous chemical deposition methods,
- 3) study of new approaches based on the use of ionic liquids,
- 4) the development of prognostic screening tools that will enable prediction of the possibility of reliability issues early in the assembly process.

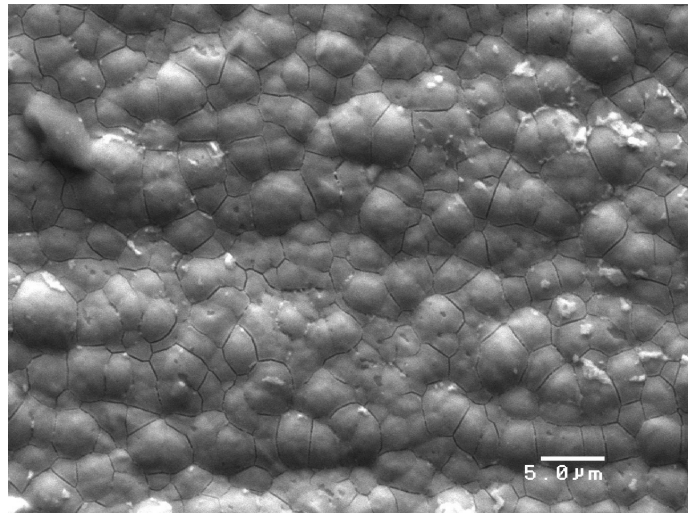
This paper introduces some of the ENIG related issues and describes progress to date on the ASPIS project.

## Nickel Gold Solderable Finishes Issues

Electroless nickel – immersion gold (ENIG) solderable finishes have long been one of the preferred finishes for protecting copper on high performance circuit board assemblies due to their excellent properties such as coplanarity, good solderability performance and compatibility with complex assembly operations. [1].

However, ENIG finishes are also known to suffer, under certain conditions, from a number of reliability issues including the so-called 'black pad' phenomenon.

The term 'black pad' is normally used to describe a problem associated with corrosion of the nickel surface that results in a loss of solderability and which can cause poorly formed solder joints at the interface between the solder and the nickel interface, see figure 1. [2].



*Fig. 1: a soldered ENIG pad after removal of the solder showing no intermetallic compound growth and the 'mud cracked' appearance of the underlying nickel often linked to 'black pad'. (Courtesy Nick Hoo, ITRI Ltd)*

These weakened joints may be dormant in an assembly, but then lead to failures when they are subjected to mechanical or thermal-mechanical stresses during operational service.

There has been much work undertaken to elucidate the mechanisms of 'black pad' formation and failure but it is still not completely understood. However, there are a number of plating factors in both the nickel and gold deposition stages that can have an influence on 'black pad' formation [3].

For example, the presence and levels of phosphorus at the surface of the nickel layer and the type of electroless nickel chemistry used can play an initial role in the occurrence of 'black pad'.

It is also possible for the immersion gold chemistry and process conditions to have an influence on the occurrence of 'black pad' and, again, there has been much work to develop new chemistries. For example, Dong et al [4] recently reported a new cyanide-free immersion gold process that can give a highly uniform gold deposit with less probability of 'black-pad' compared with that of the traditional immersion gold processes. This new approach is claimed to offer a competitive alternative to traditional cyanide-based processes, while also offering environmental benefits.

Nevertheless, there is still a need to gain a better understanding of nickel-gold deposits and the factors that impact subsequent assembled device reliability.



## Investigations of 'Black Pad' Formation Mechanisms

The excessive corrosion of electroless nickel-phosphorus (Ni-P) coatings during the subsequent immersion gold deposition process is often indicated by a grey or black appearance, ie "black pad" [5-9]. It is also well established that the corrosion properties of electroless nickel deposits are governed mainly by their phosphorus content and the corresponding structural and mechanical state [10-16]. The principal scientific objectives for the initial period of the ASPIS project have been the identification of mechanisms influencing each failure mode via experimental determination and establishment of the key factors and relationships for the failure modes identified. The following tasks were therefore undertaken:

- 1) deposition and characterization of electroless nickel coatings (phosphorus content, thickness and porosity)
- 2) corrosion behaviour studies of electroless nickel coatings in both citrate media and immersion gold solutions
- 3) characterization of gold layer (thickness, porosity and quality)
- 4) structural characterization of Ni-P samples after removal of the immersion gold layer.

Electroless nickel (EN) coatings with phosphorus contents ranging between 3.5 and 11.0 weight per cent were deposited from a glycine containing solution, while immersion layers of the required thickness (~100 nm) were deposited from a KAu(CN)<sub>2</sub> solution.

Corrosion behaviour studies were performed by applying voltammetric and electrical impedance spectroscopy (EIS) measurements. The surface morphology was examined using an SEM, while EDX and XPS were applied for determination of the surface chemical composition of the electroless nickel and immersion gold coatings. ICP was used for solution analysis.

The thicknesses of electroless nickel and immersion gold coatings were determined gravimetrically and from SEM data using 'Stratagem' software. Coating porosity was evaluated from voltammetric and EIS measurements.

All deposited EN samples exhibited nodular morphology (Fig. 2). However, several obvious distinctions in their structures were identified: the surface of the EN samples with phosphorus contents ≤ 7 wt. % were composed of spherical particles, whose size varied from 1 to 4 μm and the apparent grain boundaries were a representative feature of these coatings. The EN samples with phosphorus contents > 8 wt. % exhibited structures more typical of amorphous materials with indistinct grain boundaries and discrete spherical particles, whose size varied between 8 and 10 μm.

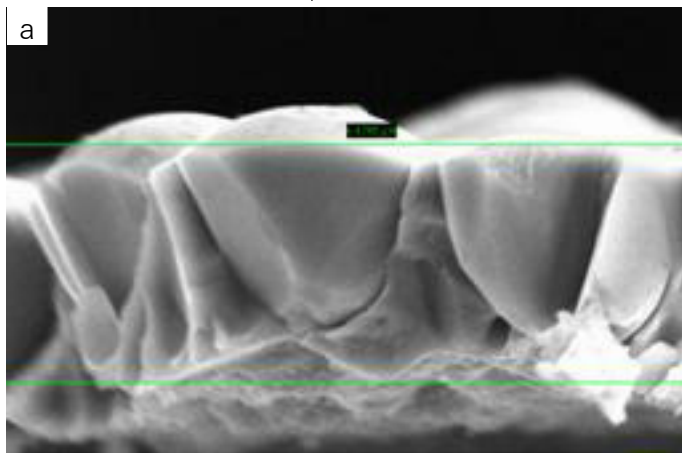


Fig. 2.a SEM images of broken edges of EN coatings:  
a - without IG layer,

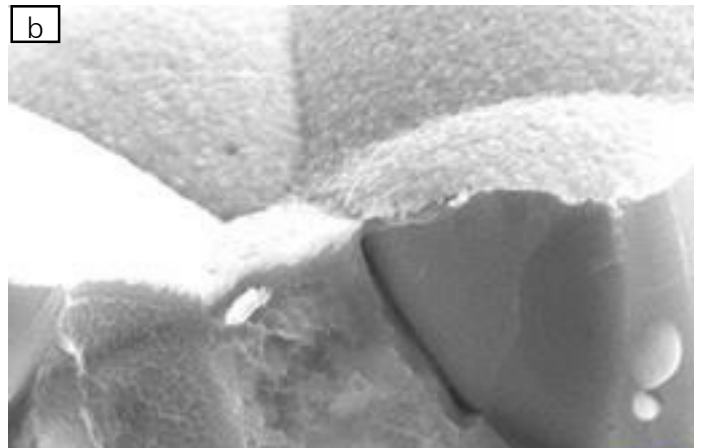


Fig. 2.b SEM images of broken edges of EN coatings:  
b - with IG layer.

Investigations of the immersion gold process revealed that the gold deposition rate was determined by the solution pH and composition and surface reactivity of EN. More reactive nickel surfaces (i.e. those with lower phosphorus contents) lead to higher plating rates in the following immersion process and increases in the amount of corrosion damage.

EDS spectra showed the presence of copper in the corroded ENIG areas. The source of this copper contamination and the role of copper on the 'black pad' formation remains unclear at the time of writing, but is being further investigated.

Possibilities include diffusion of copper atoms along nodule boundaries from the substrate and subsequent diffusion into the corroded matrix with an amorphous structure, and dissolution of the copper substrate into the immersion gold solution and subsequent contamination.

The presence of copper traces after electroless nickel exposure to the immersion gold solution was also determined by ICP analysis. Therefore, the porosity of electroless nickel coatings is one of the factors which influences the quality of the subsequent immersion gold coating and the possibility of the 'black pad' occurrence.

Attempts have also been made to elaborate a reliable and simple method for the quantitative evaluation of the porosity of electroless nickel, immersion gold and ENIG coatings, which is based on taking voltammetric measurements in a KOH solution.

For example, the porosity of an electroless nickel coating on a copper substrate was evaluated on the basis of cathodic charge consumed within the E range from 0.65 V to 0.00 V for the reduction of the copper oxides, CuO and Cu<sub>2</sub>O (Fig. 3, curve 1). This duplex cathodic peak is a well known characteristic of the electrochemical behaviour of copper in alkaline media [17]. Pores in electroless nickel coatings on copper are reflected by minor cathodic peaks within the E range of interest (Fig. 3, curve 2). Non-porous electroless nickel coatings do not exhibit such peaks (see the filled area under curve 3 in Fig. 3). In the case of porous electroless nickel coatings on copper, the portion of cathodic charge,  $Q_{EN/Cu}$ , (see the vertically patterned area between curves 2 and 3 in Fig. 3 within the E range of interest), can be treated as the measure of copper surface exposed to the electrolyte, which, in turn, is proportional to the porosity of the coating. If the charge under the cathodic reduction peaks in the cyclic voltammogram of copper electroplated on copper foil,  $Q_{Cu}$  (see the horizontally patterned area under curve 1 in Fig. 3), can be treated as 100 % copper surface, then the percentage of the surface occupied by the pores in EN coating,  $P_{EN/Cu}$ , can be evaluated according to the formula as follows:

$$P_{EN/Cu} = Q_{EN/Cu} / Q_{Cu} \cdot 100 \%.$$

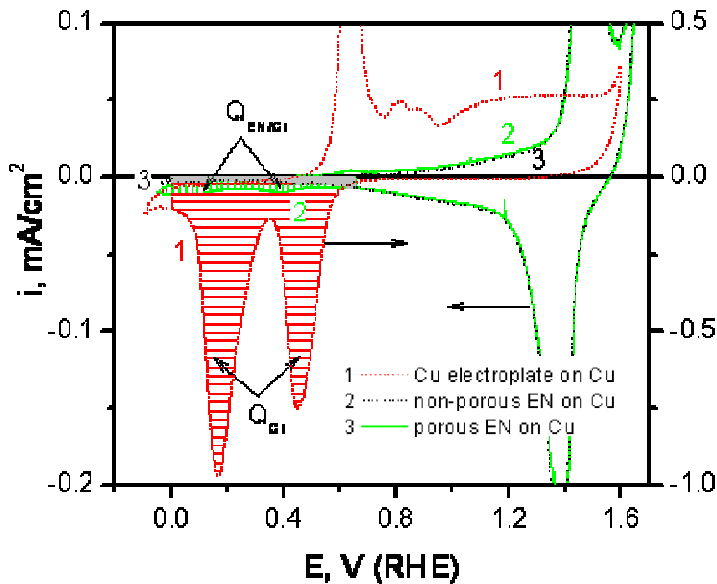


Fig. 3. Cyclic voltammograms of copper electroplate ( $\sim 5 \mu\text{m}$ ) on copper foil (right  $i$  axis) (1), porous (2) and non-porous (3) EN coatings on copper substrate (left  $i$  axis); oxygen-free solution of  $0.1 \text{ M KOH}$ ,  $v = 50 \text{ mV/s}$ .

The surface of the electroless nickel plating had a nodular structure and there were boundaries and crevices between the nodules.

Gold penetration along the electroless nickel nodule grain boundaries (Fig. 3) and other internal defects, such as spikes and cavities, were observed for this coating. If a boundary or crevice is too deep and thus the supply of gold atoms to the crevice is slowed down, the gold concentration in the crevice will be different from that of the plating bath. Consequently, a galvanic cell will be set up between the crevice and the surface, resulting in heavy corrosion in the crevice. Therefore, the corrosion converts the dense, amorphous electroless nickel into a porous, micro-crystallized structure into which the gold atoms have penetrated.

Other possible sources of weakness in subsequently formed solder joints may be the small voids found at the nickel-gold interface and impurities introduced during the immersion gold process, e.g. copper.

In the work carried out on the ASPIS project, it has been determined that the factors which favour 'black pad' formation are as follows:

- a high immersion gold bath pH value,
- a high concentration of citrate, and
- the thickness of the immersion gold layer being higher than necessary.

In addition, improper copper substrate preparation (e.g. inclusions left on the substrate surface) lead to deposition of electroless nickel coatings that may be more susceptible to 'black pad' formation. This work will continue until September 2013 and further results will be reported in due course.

#### ENIG Processing of PCB's Using Ionic Liquids

Ionic liquids (ILs) are currently of great interest within the industrial chemistry community as replacement solvents for processes that have a significant impact on the environment. ILs tend to have a benign nature, as well as low volatility, so their use has relatively little impact on the environment.[18] More importantly, due to their high salt content, they can exhibit some unusual metal speciation effects when compared to molecular solvents such as water and alcohols etc. This can have a significant impact on the way that metal ions behave in electrochemical processes.[19]

At the University of Leicester there is considerable established experience of using ILs for various forms of metal processing including electropolishing, electroplating and immersion deposition of noble metals.[20,21,22] Consequently, this experience has been exploited in the ASPIS project to investigate the potential for using these novel solvents as part of the electroless nickel and immersion gold deposition processes and to evaluate their usefulness as coatings on PCBs.

The occurrence of 'black pad' has been hypothesised to occur by galvanic corrosion of the nickel via protons in the acidic gold plating bath.[2]

The use of ILs could enable the plating bath to be neutral, minimising the extent to which this corrosion takes place and thus reducing the likelihood of 'black pad' formation.

It is also worth noting that most immersion gold processes use potassium dicyanoaurate, which can cause inherent environmental issues. The speciation properties of ILs may enable the use of a more environmentally

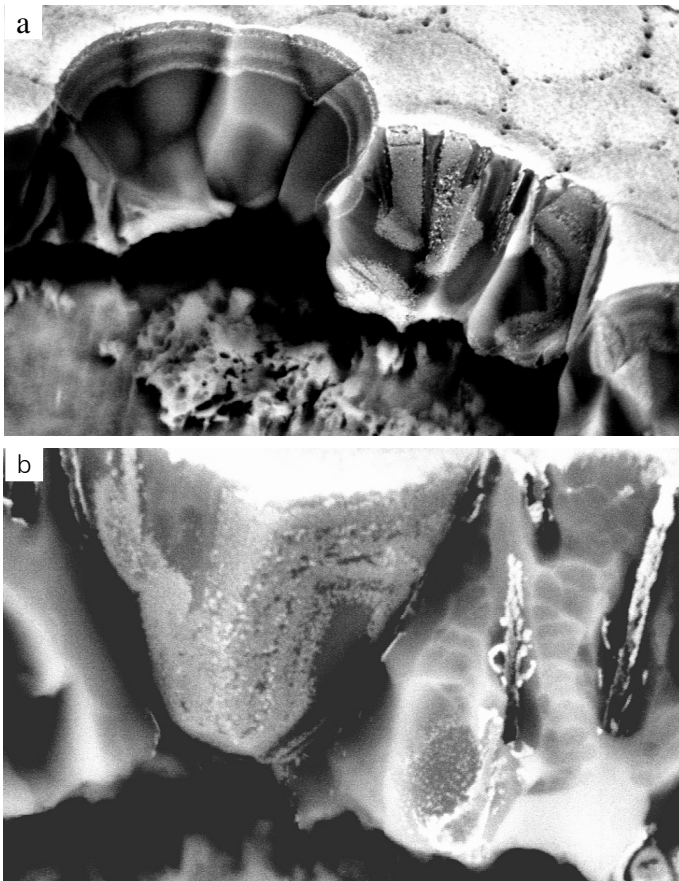


Fig. 4. SEM images of broken edges of ENIG coatings deposited in solutions containing  $0.1 \text{ mol l}^{-1}$  rate (improper copper substrate preparation).

The changes in electroless nickel surface morphology after the immersion gold process were studied by analyzing samples that were both covered with gold and ones that were stripped of gold.

A severe case of corrosion damage after immersion gold layer formation was observed on an electroless nickel sample that had been subjected to an inappropriate pretreatment process of the substrate metal (Cu) and which resulted in a highly porous structure formation.

friendly gold salt, thus reducing the subsequent treatment required for spent baths, as well as the risk to employees operating plating equipment and the overall cost of the process.

During the first year of the ASPIS project, research has been focused in two areas; investigation of silver, palladium and gold immersion coatings from ILs and the replacement of the aqueous immersion gold process with one based on an ionic liquid. There are a number of alternative coating technologies to ENIG and initial work focussed on the immersion coating of noble metals such as gold, silver and palladium onto copper. Fig 5 provides the CV data for copper (a), silver (b), palladium (c) and gold (d) in the ionic liquid Ethaline 200. The CVs show that the galvanic deposition of silver, palladium and gold are thermodynamically favourable with respect to the Cu/Cu<sup>+</sup> redox couple. Additionally, gold immersion coatings onto silver and palladium are also thermodynamically favourable in these liquids.

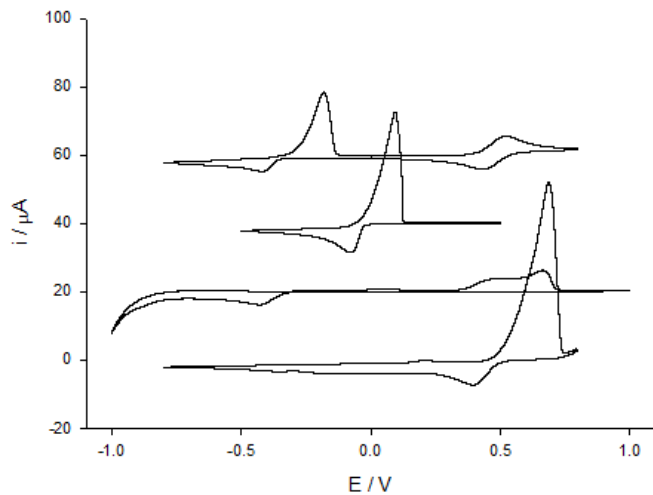


Fig. 5: Offset cyclic voltammograms of metal salt / Ethaline 200:  
 (a) 0.02 M CuCl, offset + 60  $\mu$ A,  
 (b) 0.02 M AgCl, offset + 40  $\mu$ A,  
 (c) 0.02 M PdCl, offset + 20  $\mu$ A,  
 (d) 0.02 M AuCl. Electrodes: working - 2 mm Pt disc, counter - Pt flag, reference - Ag wire.  $n = 10$  mV s.

Copper has been successfully coated with gold, silver and palladium. Furthermore, a secondary coating of gold has been successfully coated on to both silver and palladium coatings. The morphology of these coatings has been found to be dependent on the substrate, mimicking the morphology already present, producing uniform, bright, non-porous coatings.

Copper mobility has been demonstrated in the gold coating, highlighting the need for a barrier layer between gold coatings and copper substrates. Palladium has also displayed some copper mobility, but significantly less than gold.

In the gold coating of palladium, the palladium slowed the copper migration, but did not prevent it. Silver coatings showed a very slow copper migration, lower than both the palladium and gold coatings.

Gold coatings on silver, however, showed a higher copper migration than just a silver coating. This suggests that silver is not a suitable barrier layer between copper and gold, however it is an excellent coating for PCBs in its own right.

Initial development work has also been carried out on immersion gold coating depositions from ILs onto an electroless nickel surface that was produced from a

standard aqueous nickel sulphate and sodium hypophosphite solution.

In an effort to remove the most significant hazard from this process, the KAu(CN)<sub>2</sub> has been replaced with AuCl. AuCl is known to disproportionate to Au metal and AuCl<sub>3</sub> in aqueous solutions and, consequently, this is a deposition method that is possible via the use of ILs in this research.[23].

Initial experiments involved the deposition of gold from AuCl Ethaline 200 solutions at varying concentrations and temperatures. The gold was found to deposit quickly with a bright coating covering the whole of the gold surface in under 20 minutes from a 0.1 M AuCl solution at 50°C.

Figure 6 shows the surface (a) and cross section (b) SEM images of an aqueous electroless nickel/ionic liquid immersion gold sample. Figure 6 (a) shows the presence of a good overall coating of gold on the surface, with the nodular structure characteristic of an electroless nickel surface still visible while Figure 6 (b) shows that the approximately 4.5  $\mu$ m nickel has been coated with a thin but even covering of gold across the whole of the sample, which can be seen as the thin bright line indicated by the arrows.

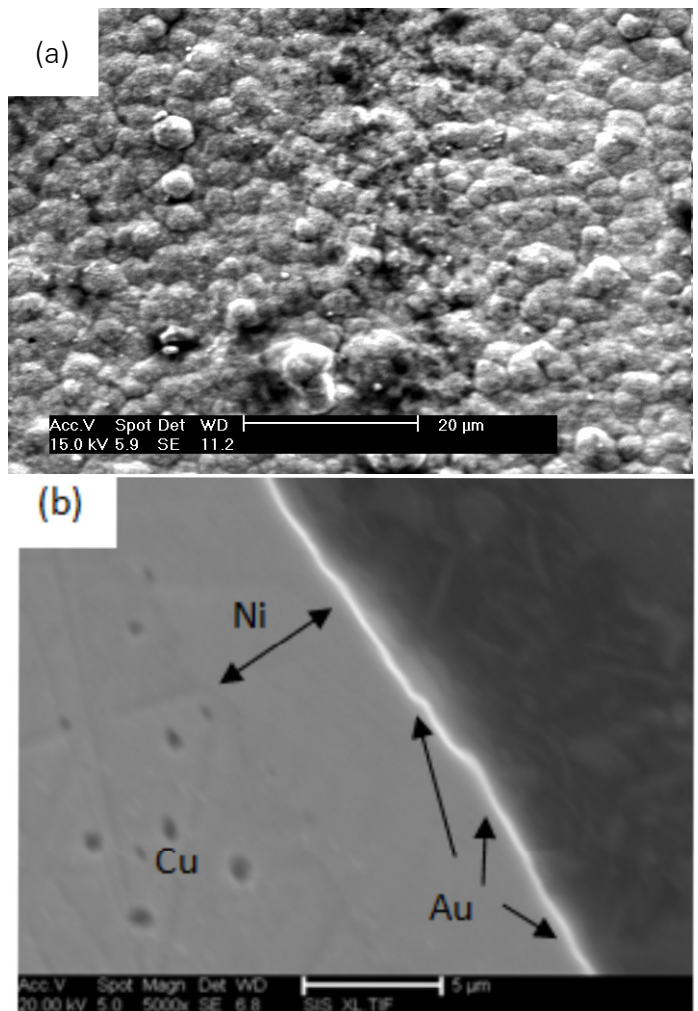


Fig. 6: The surface (a) and cross section (b) SEM images of immersion gold from AuCl in Ethaline 200 onto electroless nickel from aqueous solution.

EDX analysis revealed that these samples indicated the presence of a moderate amount of copper within the sample (30 atomic% copper compared with 70 atomic% gold) and this has been attributed to the presence of a



bare copper surface where copper is oxidised in place of nickel and co-deposited with gold.

Work with AuCl in Ethaline 200 on samples that did not have any bare copper present provided poorly adhesive deposits. This was likely to be due to the slow kinetics of nickel oxidation within these liquids.

Further work is underway to investigate the addition of higher field ligands to these solutions such as thiosulfate, nitrite and ethylenediamine, which should slow the kinetics of gold reduction, providing higher quality, more reliable finishes. Initial results have been very positive and these will be reported at a later date when further work has been completed.

Over the next year, work will continue on optimisation of the process and further analysis will be conducted on gold immersion coatings from ILs, as well as the development of an electroless nickel deposition process from ionic liquids.

### Development of an ENIG Screening Tool

Another key objective of the ASPIS project is the development of an ENIG screening tool. Since there is still much debate about the definition of 'black pad' and the mechanisms which influence its occurrence, an initial aim was to gain a detailed understanding of this phenomenon and of the forms in which it can appear.

To achieve this objective, an initial literature study was conducted based on more than thirty papers that dealt with either 'black pad', or ENIG plating defects in general.

From this study, an inventory of ENIG plating defects was compiled and documented in a FMEA (Failure Mode Effect Analysis). In the next step, actual ENIG plating defects were analysed in order to study appearances and to determine more about their detectability. Defective printed circuit boards were provided by ASPIS partners and a customer of TNO Technical Sciences. SEM-EDX, XRF, confocal microscopy and chemical testing have been used, as appropriate, to analyse bare boards, solder joints and cross-sections.

Distinguishing 'black pad' from other similar issues can be a challenging task. Fig. 7 shows an example of an issue encountered at a Ball Grid Array (BGA) component soldered on an ENIG board. Early field failures occurred due to the rather low drop impact resistance of the solder joints. By cross-sectioning and analysing each fractured side of the joint, it could be determined that the solder joints fractured between the Ni-P and the intermetallic layer.

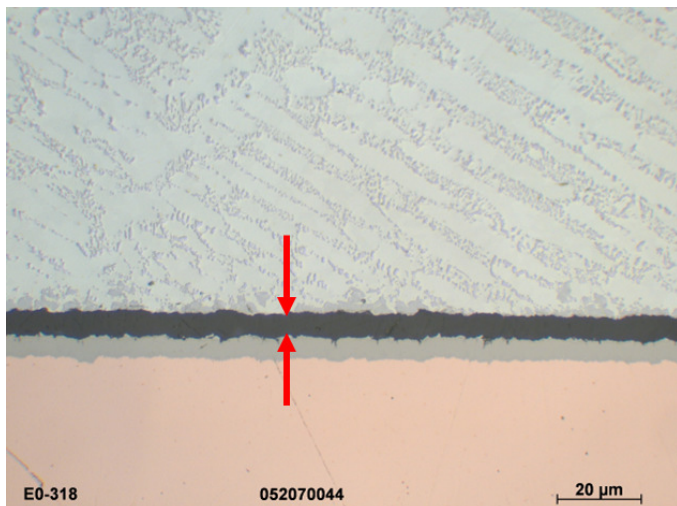


Fig. 7: Fracture between the Ni-P and the intermetallic layer.

Figure 8 shows another BGA solder joint cross-section coming from the same series. In this case, the PCB solder interface was still intact, but a region with small dark spikes was also present at the topside of the nickel layer.

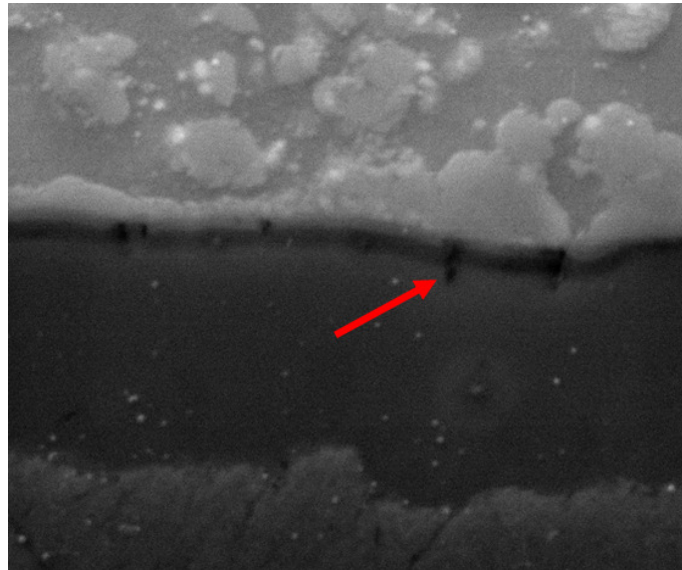


Fig. 8: Small dark spikes on the topside of the nickel layer (SEM, 25 kV, 10,000x).

This may be an indication of an early stage of a corrosion related to the occurrence of issues such as 'black pad'.

Another indication was the detection of copper, by SEM-EDX, at the surface of unsoldered pads. Since other contaminating elements were also detected next to this, a further and more detailed examination would be desirable.

Fig.9 shows an example of different surface morphologies detected on a PCB with randomly discoloured ENIG pads due to a skip plating problem.

Since changes in surface morphology are also expected with 'black pads', surface inspection techniques are considered to be a useful option for distinguishing 'black pad' and will be further developed later project.

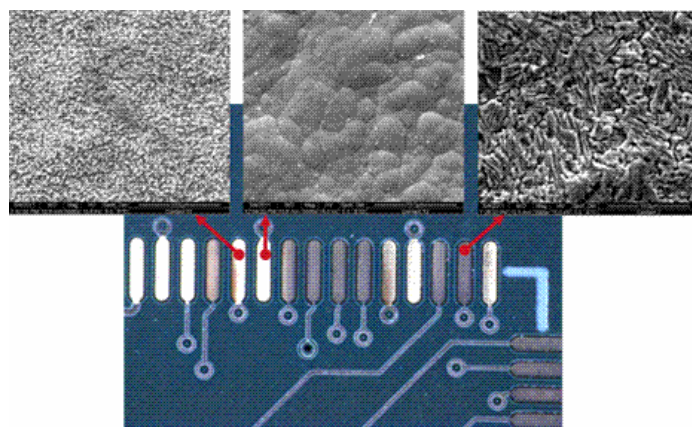


Fig. 9: Surface morphologies of different ENIG pads in the same footprint (SEM, SE, 15kV, 5000x).

Fig. 10 shows the results of elemental analysis (EDX) performed with different acceleration voltages at the same location. This experiment indicated that the copper detected through the immersion gold layer was present at the top side of the nickel layer. (Increasing the acceleration voltage from 15 kV to 25 kV resulted in a decrease in copper content.) Copper diffusing along nickel nodules to the top surface of the nickel layer is a known 'black pad' related side effect.

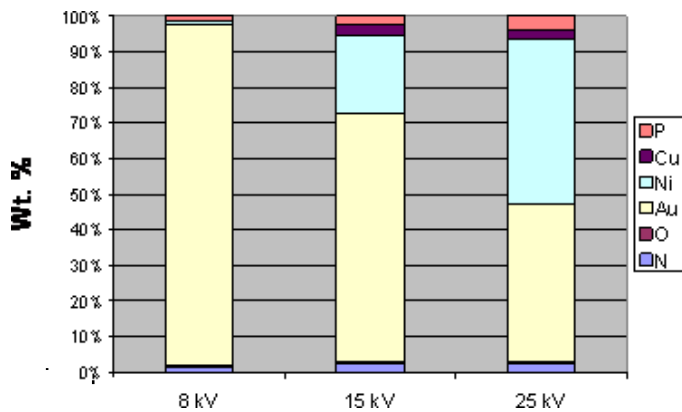


Fig. 10: Element analysis (EDX) at the top surface of a pad conducted at different acceleration voltages

As the main aim of this part of the ASPIS project is the development of a screening tool, an inventory of currently available inspection techniques has been made. Together with an inventory of possible new strategies, this work has resulted in a better understanding of the available non-destructive inspection techniques that may be applicable.

To investigate whether the screening tool should help to remove potential causes, and control failure mechanisms or improve the detectability of failure modes, a QMAP (Quantitative Method for Analysing Production Processes) has been conducted to analyse the design, PCB manufacturing and assembly stages.

At each stage the parameters, together with potential available control mechanisms, have been systematically considered to give direction to the development of an effective detection approach. Work is continuing on the development of the screening tool and the results will be reported in a future publication.

### Summary and Conclusions

This paper has reported some of the initial progress made, and results obtained, during the first year of the three year European funded ASPIS project, which is seeking to gain a better understanding of the mechanisms influencing the performance of nickel-gold coatings and to develop new aqueous and non-aqueous chemistries that will give enhanced performance and reliability. The project is continuing until September 2013 and further progress reports on the work undertaken will be made in due course. Additional information about the ASPIS project can be found at [www.aspis-pcb.org](http://www.aspis-pcb.org).

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# Peter Starkey

reviews papers presented at the  
**ICT Symposium - "Supporting Industry Needs"**  
1st November 2011  
Devonport Hotel, Darlington

The night was drawing in as I made the long drive to the north-east of England for the Institute of Circuit Technology 2011 Darlington Seminar on November 1st. British Summer Time had ended the previous weekend and at 5pm it was already too dark to see the autumn colours of the trees and hedgerows on the banks of the River Tees.

But on the bright side, ICT Technical Director **Bill Wilkie** had once again organised an excellent programme which attracted an attentive crowd of PCB fabricators and suppliers, and he introduced the seminar with the encouraging news that membership of the Institute continued to grow steadily and that events were increasingly well-supported.

First to present was **Geoff Layhe**, Technical Manager at **Lamar Group**, who explained how the technical demands of the rapidly growing market in LED lighting had driven the development of white solder mask inks specifically for high-luminance LED applications.

The main challenge to be overcome was the discoloration of standard white solder mask by heat and UV exposure. Epoxy resins used for conventional high-performance solder masks had a natural tendency to discolour when subjected to sustained high temperatures.

In cooperation with major LED OEMs, Taiyo Ink, who supplied over 45% of the world solder mask requirement, had carried out extensive studies of materials and formulations and introduced a new range of liquid photoimageable solder masks with high reflectance and resistance to UV and thermal discoloration.

Their PSR-4000 LEW3 was the highest performing LED solder mask in terms of reflectance and discoloration, and Layhe showed test results that indicated its superior properties. He made some interesting practical observations on staining effects after gold plating. If pink or purple stains appeared on a white solder mask, this was an indication of inadequate rinsing, resulting in a subsequent chemical reaction between residues of gold salts with the titanium pigment in the mask.

As well as their range of white solder masks, Taiyo had introduced a white ink-jet marking ink which had become widely accepted and had been adopted as standard for Orbotech's Sprint printers.

**ICT Chairman Professor Martin Goosey** reported on two EU-funded projects: **ASPIS** and **SUSONENCE**.

The **ASPIS** Project, aimed at enhancing the performance of nickel-gold solderable finishes, had been running for one year and had already produced some interesting data on the fundamental characteristics of the electroless nickel deposition process, particularly the effects of pH on deposition rate, phosphorus content, deposit morphology and grain-boundary characteristics.

It had also been established that corrosion of the nickel surface was due to activity in the immersion gold process, and a high gold-bath pH together with a high citrate concentration was a combination of parameters which encouraged black-pad formation.

Nickel deposition from ionic liquid chemistries offered a possible route to avoid the co-deposition of phosphorus, a by-product of the reducing agent in conventional chemistry and a known contributor to the black pad effect.

ICT had the responsibility for training, exploitation and dissemination of the outcome of the programme. Papers had been published in industry journals and a website was operational at [www.aspis-pcb.org](http://www.aspis-pcb.org).

**SUSONENCE** was a new FP7 eco-innovation project originating out of work supported by IeMRC and directed at the development of sustainable, ultrasonically enhanced surface modification processes to reduce chemical usage and decrease waste and environmental impact in the PCB and metal finishing industries, particularly in the areas of removing surface layers, etching and texturing of widely-used substrates.

**Mike Partridge**, MD of **Lamar Group** gave a very informative presentation on the mechanism and benefits of contact cleaning, with many hints and tips on how to maximise the effectiveness of the process, which had a wide variety of particle-removal applications in PCB manufacture.

These typically included cleaning of laminates, prepregs, conformal films, press plates, artworks, exposure frames, boards prior to testing or assembly, and even clean-room walls and floors.

Partridge discussed the critical attributes of elastomer rollers, which were available with different hardness values to suit particular applications, and adhesive transfer rolls. He described the principles of operation of panel-cleaning machines, which were often not fully appreciated, listed what types of contamination they would and would not remove, and advised how simple basic maintenance procedures could improve consistency of performance.

There were many other industries where contact cleaning was employed to good effect and, as an illustration, Partridge explained how a dramatic yield improvement had been achieved in the manufacture of lorry windscreens by the introduction of contact cleaning, with the initial investment paid back after only 2½ days!

**Deputy Chairman of the ICT** and Head of Materials at **Coventry University's Sonochemistry Centre**, **Dr Andy Cobley** described the effects of ultrasound on the electroless copper plating process, being studied as part



of the ULTElmet Project, funded by the Engineering and Physical Sciences Research Council via **leMRC**.

It had been observed that ultrasound had an apparently negative effect on plating rate at temperatures below 35°C and a slightly positive effect above 35°C. Very low or very high frequency tended to de-stabilise the electroless copper; and best results were obtained at frequencies near 40kHz.

But the negative effect on plating rate had been found by x-ray photoelectron spectroscopy to correspond with the displacement of palladium catalyst from the activated surface, and the effect could be overcome by delaying the application of ultrasound to enable the electroless reaction to initiate without disturbance of the catalyst. Significant improvements in plating rate were then observed.

An ecological objective of the project was to achieve acceptable plating rates with non-formaldehyde reducer chemistries. In addition to its effect on plating rate,

ultrasound improved the morphology of the electroless copper deposit, with finer grain size and reduced porosity.

At the conclusion of the technical proceedings, delegates enjoyed a splendid buffet supper, courtesy of Lamar Group whose generous support of the event was gratefully acknowledged, and constructive conversation continued late into the evening.

Thanks to Bill Wilkie's unstinting endeavours, the regional evening seminar is now established as an essential meeting place for everyone interested both in keeping in touch with developments in printed circuit technology and in sharing experiences with their counterparts in the industry.

**Pete Starkey**

ICT Council



Geoff Layhe,

Andy Cobley,

Martin Goosey

Mike Partridge.



# Peter Starkey

reviews opinions presented at the  
**PCB Nickel-Gold Surface Failures:  
the Good, the Bad and the Ugly Webinar**  
9th November 2011

PCB Nickel-Gold Surface Failures: the Good, the Bad and the Ugly Seminar – not an ageing spaghetti western produced by Sergio Leone and starring Clint Eastwood but a state-of-the-art technical webinar on a significant industry issue, produced by Bob Willis and starring leading authorities in the field of printed circuit materials, manufacture, test and trouble-shooting:

**Nigel White** from Atotech,  
**Dennis Price** from Merlin Circuit Technology,  
**Dr Chris Hunt** from the National Physical Laboratory  
**Professor Martin Goosey**, Institute of Circuit Technology

**Bob Willis** put the topic into context with statistics from SMART Group web surveys indicating that, of the PCB defects reported by users, solderable finish faults accounted for more than 35% of the total. Then, with reference to IPC acceptability specifications IPC-A-600, IPC-A-610, the IPC Test Methods Manual, J-Standards and solderable surface finish standards IPC-4552, IPC-4553 and IPC-4554, he showed a series of photographs illustrating many examples of PCB assembly process problems including surface non-wetting, black tarry pads, solder finish lifting, nickel-gold tape-testing failures and BGA-package-to-PCB separation.

Willis then handed over to **Nigel White**, who gave an introduction to electroless-nickel-immersion-gold technology from the perspective of the process supplier, beginning by listing the attributes expected by the industry:

- multiple soldering capability for both tin-lead and lead-free processes,
- aluminium wire bondability,
- constant contact resistance for keypads and switches,
- planarity,
- a phosphorus content in the range 7-10%, and a 12-month shelf life.

ENIG was a two-stage metal deposition process, where the nickel-phosphorus functioned as a diffusion barrier and added strength to plated-through holes and vias.

The solder joint was actually formed as a tin-nickel intermetallic. The thin gold layer minimized the interaction of nickel with the environment and was dissolved in the solder.

ENIG was a mature process, which had been used since the early 1990s. The reaction mechanism involved the deposition of a nickel-phosphorus on a palladium-sensitised copper surface by autocatalytic reduction, followed by the semi-autocatalytic immersion deposition of gold on the nickel surface.

White described the process in detail, including some available options to overcome problems such as the entrapment of chemistry in partially plugged via holes, and some notes on process performance and deposit characteristics.

Concerns and limitations were :-

- the cost of precious metal,
- the potential brittleness of the tin-nickel intermetallic,
- corrosion of nickel by the immersion gold solution,
- the tight process control required
- and the unsuitability of ENIG for gold wire-bonding applications.

But on the positive side, ENIG was suitable for :-

- multiple lead-free soldering,
- it had planarity to suit surface mount component placement requirements,
- and the nickel barrier layer prevented dissolution of copper by solder.

It also exhibited:-

- good shelf life,
- good resistance to corrosive environments,
- presented a good surface for ICT probing and contact switching applications
- and was suitable for aluminium wire-bonding

Nigel White having described ENIG from the supplier side, **Dennis Price** gave a user view based on his many years of practical experience at **Merlin Circuit Technology** in controlling and optimising the performance of the process.

He emphasised the importance of proper copper surface preparation prior to the application of solder mask: Merlin's preferred method was low-pressure pumice scrubbing with nylon-bristle brushes.

Price gave a word of caution regarding solder mask adhesion failure: in the past, many fabricators had attempted to overcome major adhesion problems by initially only part-curing the solder mask to retain flexibility during ENIG processing, with apparent success but with the consequence that sulphur-containing compounds were leached out and contaminated the nickel bath.

Price went through Merlin's 23-step process sequence stage-by-stage, with hints, tips and observations, stressing the relevance and importance of meaningful laboratory analysis, data recording and statistical process control.

One of the main causes of skip plating was, as Nigel White had commented, entrapment of micro-etch solution in partially-closed via holes, which could bleed out and poison the palladium activator on local features.

Extraneous nickel deposits could result from wicking of activator into the cut ends of glass yarns in non-plated holes or the activation of trace residues of un-etched copper metal in the laminate surface.

Although it could appear attractive to run electroless nickel baths for many metal turnovers to reduce process costs, it had been shown that the increased concentration

of contaminants and by-products could result in nickel deposits which were more prone to surface hyper-corrosion during the plating of immersion gold.

Price also underlined the importance of topping-up of evaporation losses by little-and-often additions, and advocated the use of an automatic controller for the electroless nickel plating bath, which could continuously monitor nickel concentration and made additions of nickel and hypophosphite replenishers in small increments to maintain the chemistry within close working limits with a minimum of operator dependence.

After the comprehensive chemistry lessons came a presentation on PCB failure analysis techniques from **Chris Hunt**, who described how defects were identified and failure mechanisms studied and interpreted, using the wide range of test and inspection techniques available at **NPL**, including optical, x-ray and scanning electron microscope examination, microsectioning, x-ray fluorescence spectroscopy, shear testing and hot pull testing, illustrated with many examples.

He gave details of the Defect Database on printed board assembly and material issues, managed by the **NPL Electronics Interconnection Group** as a service to the electronics industry. Any visitor to the database could add defect information and photographs from his own observations, and have free access to the continuously increasing catalogue of reference data and images to assist in implementing corrective actions in processes or designs.

Next to speak was **Martin Goosey**, who was coordinating a **three year EC Framework 7 project** known as **ASPIS** - Advanced Surface Protection for Improved Reliability PCB Systems. The ASPIS project aimed to develop new, more reliable materials, processes and testing procedures in order to address the key issues associated with ENIG finishes.

The project had adopted a number of technical approaches ranging from an in-depth study of the fundamental mechanisms that influence the metal deposition and subsequent reliability, to the development of new chemical processes based on both traditional aqueous chemistry and new ionic liquids. In addition, work was being carried out to develop better methods for identifying failure mechanisms and a non-destructive prognostic screening tool that could be used to give warning of latent problems on printed circuit boards in advance of components being soldered on to them.

Progress to date included the demonstration of nickel and gold deposition from novel ionic liquid-based chemistries, and a more detailed understanding of the key factors influencing the formation of "black pad" defects.

**Bob Willis** gave the final presentation "**BGA Joint Inspection Using Dye & Pry Testing – How to Do It Yourself**".

The dye-and-pry technique was useful as a means of detecting subtle open circuits caused by wetting problems on pad surfaces or flexing of the BGA or the PCB during reflow. On ENIG-finish PCBs, as the solder paste fused it would dissolve the gold and apparently wet the pad, but could still fail to form a sound intermetallic bond to the nickel, and this type of defect was very difficult to detect by traditional methods of optical or x-ray inspection or electrical test. Dye penetrants had been used for many years in the testing of welded joints and castings prior to destructive analysis, and Willis explained how they could be used as the basis of a low-cost alternative test to quickly and straightforwardly reveal the location of a failure in a BGA assembly. In practical terms, the procedure was to impregnate the suspect area with a proprietary dye, using vacuum assistance if possible, dry it in an oven then pry off the component with a chisel and examine the remains of the joints for evidence of dye penetration. As usual, he provided an abundance of

pictorial illustrations, and explained in detail how to interpret and record the results.

*The Good, the Bad and the Ugly Seminar proved to be an informative and educational event. Three hours is a long time to hold peoples' attention but Bob Willis did a very professional job of maintaining the continuity of the programme and moderating the real-time question-and-answer session, which generated some highly interactive dialogue and exchange of ideas and experiences.*

Pete Starkey

I-Connect007  
November 2011

To view Videos of the Webinar go to :-

[www.instct.org/seminar-reports](http://www.instct.org/seminar-reports)

This is a members only benefit and if you are not logged in you will only see the public version.



# Innovative Electronics Manufacturing Research Centre (leMRC)



**Martin Goosey**

leMRC Industrial  
Director

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## New R&D funding support announced by the UK's Innovative Electronics Manufacturing Research Centre (leMRC)

During October 2011, the UK's Innovative electronics Manufacturing Research Centre (leMRC) announced that it was awarding more than £1.5 million in funding to support five new research projects at key universities around the country. Following a recent call for proposals and an initial filtering stage, selected proposals were subjected to an international peer review process after which five projects were subsequently chosen to receive funding support. The successful proposals were from the universities of Bath, Birmingham, Coventry, Nottingham and Southampton. All of these new leMRC-funded projects are closely engaged with industry in the development of new products, processes, industry practices and an increasingly valuable skills base that can support high value manufacturing in the UK.

Launched in October 2004, the leMRC supports research that is specifically aimed at meeting the future needs of the UK's electronics industry.

The newly funded work that will be undertaken at **Bath University** focuses on helping companies manufacturing large infrastructure, high-value electronic systems that are facing the challenge of changing market structures. They are increasingly required to provide services and product service systems, as opposed to offering products in a development that has been described as 'servitisation'. This leaves them with a high level of uncertainty due to the novelty of the process and the long-term nature of the services that must be provided. This uncertainty is intensified by global competition and the pressure for high productivity to secure competitive advantage. The aim of this new leMRC supported project is to provide electronic product-service integrators with a tool to assist in the decision of contract pricing to win future design, manufacture and operations and support contracts for large infrastructure, high-value electronic systems. It is also expected to define a process for the facilitation of this support in the form of a decision matrix which includes the probability of winning a contract, the probability of making a profit and the expected value of this profit.

**Birmingham University** has an established reputation for its work on the high resolution resists that are used for patterning materials such as silicon. Silicon is relatively easy to produce and process using photolithography techniques and rapid progress in silicon micro-fabrication has led to the development of an increasingly diverse range of non-electronics micro and nano-products. Examples include microsensors and actuators, microfluidic systems and self-cleaning surfaces.

To date, micro and nano-fabrication has been completely dominated by techniques and materials initially developed for silicon. However, the component industry is pushing to sub-micron feature sizes and is limited by optical resolution. In particular, applications such as metal oxide on glass patterning are of significant interest to companies in this area and would greatly benefit from enhanced resolution and accuracy. It has proved extremely challenging to adapt established micro-fabrication methods to poor conductors, such as glass and GaN. Electron Beam Lithography (EBL) is particularly well suited to high value/low volume nano-device manufacture but, for glass and GaN, which are very poor conductors, the use of EBL leads to problems as the electrons in the beam cause substrate charging and distortion of the lithography pattern.

The leMRC-funded project at Birmingham University will create new high speed and high resolution electron beam resists that are also conductive. This will prevent charging related pattern distortion and the new resists will enable significant advances in electroforming on glass and GaN manufacturing. They will also find use in diamond electronics and plastic nanopatterning.

The UK electronics industry is dominated by SMEs and the manufacturing processes they use must become more cost effective and efficient if they are to compete with the low cost economies of the world. An underpinning technology within the electronics industry is the requirement to metallise dielectric materials to form conductive tracks and interconnections on a range of materials such as PCBs, RFID tags and plastics. One of the most common methods of metallisation is electroless plating, which utilizes precious metals. However, these are problematic in terms of expense, scarcity and resource efficiency. The R&D costs associated with developing new metallisation processes are also significant and the large corporate suppliers are reluctant to invest in developing 'precious metal-free' metallisation processes. There is therefore a gap between what is required by SMEs and what is provided by their suppliers.

The research programme that the leMRC is supporting at **Coventry University** (in collaboration with **Loughborough University**) will seek to fill this gap by producing low cost metallisation processes that are applicable to the high value electronic manufacturing sector. The project will functionalise copper nanoparticles (CuNP) by attaching molecules to modify their surface properties. This functionalisation will enable them to attach to a range of substrates to act as a catalytic seed layer for electroless metallisation and to be a replacement

for the more expensive palladium. In this project the functionalised CuNP will also be utilized as a conductive film for the 'direct' electroplating of through holes and vias of PCBs. In addition, the project brings together two successful groups from the leMRC community in the Sonochemistry Centre at Coventry and Loughborough University.

Power electronics is a £70 billion direct global market, growing at a rate of 11.7% per annum and is a key thematic area underpinning much of the leMRC's work. It is essential to all future sustainable energy scenarios and is thus a critical technology for a large proportion of UK industry. Despite this importance, there is increasing evidence that many power electronic devices and systems are unsuited to the stringent demands of energy and transport applications. For example, offshore wind farms and electric vehicles, where unpredictable, fluctuating loads and exposure to widely varying environmental conditions present a particularly challenging environment. Reliability design methods applied to power electronic modules are currently unable to capture the complex nature of such loads and additionally, do not account for the micro-structural evolution of bonding and interconnect materials during degradation, which further restricts their application. Resulting designs thus tend to be conservative, leading to high capital costs and low confidence in predictions of in-service life. The aim of the leMRC project being funded at **Nottingham University** is to extend physics-of-failure-based wear-out models and associated robustness design and health management methodologies to meet the requirements of power electronics in future transport and energy systems. The project will commence with the development of damage mechanics based models for key bonding and interconnect technologies that include the effects of microstructural changes - for example - due to thermal exposure. These new damage models will be incorporated into time-domain physics-of-failure models which can accurately reflect the influence of arbitrary loading. A risk-based approach to reliability prediction will take account of uncertainties in the manufacturing processes, including material properties and geometry etc. Nottingham will also enhance its fusion-based prognostics approach for power electronic assemblies to include the latest physics of failure models to monitor power module material degradation and remaining useful life, both during qualification testing and in the field.

Electrical contacts are often the weakest link in electrical and electronic systems and, as engineering systems become increasingly complex, with ever greater numbers of embedded electronics, sensors and actuators, this issue is becoming more important. There is thus a growing opportunity for innovative solutions using emerging material systems combined with innovative design approaches stemming from a fundamental understanding of the mechanisms determining contact performance. The research project being supported at **Southampton University** is focused on low current electro-mechanical (EM) switching devices, which are core to a wide range of systems. The key advantages of EM devices over solid state devices are electrical isolation, lower losses, smaller volume, lower cost and higher current handling capability per unit volume. The new project is focused on MEMS (Micro-Electro-Mechanical Systems) relay devices where the requirement for a large number of switching cycles with minimal interface wear or degradation is particularly demanding. A solution to this problem has the potential to have a profound impact on a range of electrical and electronic applications, for example, in consumer electronics as power control devices to extend battery life or in RF MEMS switching. The project will investigate new composite surfaces and will include a full investigation of their physical properties. Understanding of the contact and impact mechanics and the conduction mechanisms (both thermal and electrical) will allow the optimisation of these surfaces. Optimisation will also enable new manufacturing processes to be established and applied in the manufacturing of MEMS switching devices.

The five projects being supported by the leMRC, and briefly outlined above, will strengthen the leMRC's overall portfolio of research. It is expected that the outcomes of this research will ultimately offer real benefits to the UK's electronics industry. The leMRC is planning to announce one more call for proposals within its current round of funding and this is likely to take place during the first part of 2012. Further information about the leMRC, its work and related activities can be found at [www.lemrc.org](http://www.lemrc.org).

**Martin Goosey**  
leMRC Industrial Director  
October 2011

| <i>Organisation</i>                              | <i>Address</i>  | <i>Communication</i>  |
|--|---|---|
| <b>Anglia Circuits Ltd.</b>                      | Burrel Road, St.Ives, Huntingdon<br>PE27 3LB                                | 01480 467 770<br><a href="http://www.angliacircuits.com">www.angliacircuits.com</a>           |
| <b>Atotech UK Ltd.</b>                           | William Street, West Bromwich.<br>B70 0BE                                   | 01210 067 777<br><a href="http://www.atotech.de">www.atotech.de</a>                           |
| <b>CCE Europe</b>                                | Wharton Ind. Est., Nat Lane, Winsford<br>CW7 3B                             | 01606 861 155<br><a href="http://www.ccee.co.uk">www.ccee.co.uk</a>                           |
| <b>Electra Polymers Ltd.</b>                     | Roughway Mill, Dunks Green, Tonbridge<br>TN11 9SG                           | 01732 811 118<br><a href="http://www.electrapolymers.com">www.electrapolymers.com</a>         |
| <b>The Eurotech Group</b>                        | Salterton Industrial Estate, Salterton Road<br>Exmouth<br>EX8 4R            | +44 (0) 1395 280100<br><a href="http://www.eurotech.com">www.eurotech.com</a>                 |
| <b>Falcon Group</b>                              | Riverside Ind. Est. ,Littlehampton<br>BN17 5DF                              | 01903 725 365<br><a href="http://www.falconpcbgroup.com">www.falconpcbgroup.com</a>           |
| <b>Faraday Printed Circuits Ltd</b>              | 15-19 Faraday Close, Pattinson North Ind. Est.,<br>Washington.<br>NE38 8QJ  | 01914 153 350<br><a href="http://www.faraday-circuits.co.uk">www.faraday-circuits.co.uk</a>   |
| <b>Graphic plc</b>                               | Down End, Lords Meadow Ind. Est.,<br>Crediton<br>EX17 1HN                   | 01363 774 874<br><a href="http://www.graphic.plc.uk">www.graphic.plc.uk</a>                   |
| <b>GSPK (TCL Group)</b>                          | Knaresborough Technology Park, Manse Lane<br>Knaresborough<br>HG5 8LF       | + 44 (0)1423 798 740<br><a href="http://www.gspkcircuits.ltd.uk">www.gspkcircuits.ltd.uk</a>  |
| <b>Invotec Group Ltd</b>                         | Hedging Lane, Dosthill ,<br>Tamworth<br>B77 5HH                             | 01827 263 000<br><a href="http://www.invotecgroup.com">www.invotecgroup.com</a>               |
| <b>Rainbow Technology Systems (The TH Group)</b> | 40 Kelvin Avenue, Hillington Park<br>Glasgow                                | 01418 923 320<br><a href="http://www.rainbow-technology.com">www.rainbow-technology.com</a>   |
| <b>Stevenage Circuits Ltd</b>                    | Caxton Way, Stevenage.<br>SG1 2DF   | 01438 751 800<br><a href="http://www.stevenagecircuits.co.uk">www.stevenagecircuits.co.uk</a> |
| <b>Teknoflex Ltd</b>                             | Quarry Lane,<br>Chichester<br>PO19 8PE                                      | 01243 832 80<br><a href="http://www.teknoflex.com">www.teknoflex.com</a>                      |
| <b>Ventec Europe</b>                             | 12A Longfield Road Sydenham Industrial Estate<br>Leamington Spa<br>CV31 1XB | <a href="http://www.ventec-europe.com">www.ventec-europe.com</a>                              |
| <b>Zot Engineering Ltd</b>                       | Inveresk Industrial Park Musselburgh,<br>EH21 7UQ                           | 0131-653-6834<br><a href="http://www.data@zot.co.uk">www.data@zot.co.uk</a>                   |

## The Membership Secretary's notes - January 2012



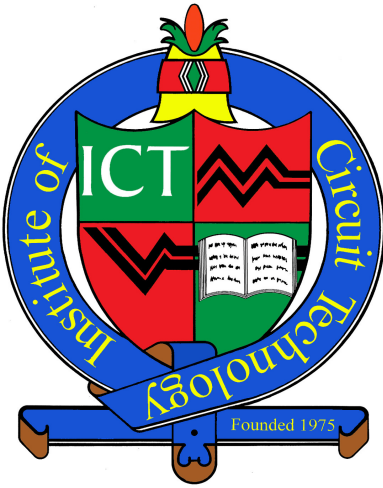
I have to start this section with a negative note, in reporting that the 2014 World Conference will be held in Nuremberg and not London as was hoped. It is a bit of a disappointment, but it leaves us free to promote other events, such as the growing National Electronics Week (NEW) in Birmingham, to be held next April.

On a much more positive note, the ICT Membership Register stands at over 260, with 15 Corporate Members.

This much improved situation is due to a lot of hard work among the Council in getting our message to the Industry. Although most of our Membership continue to be in the Fabricator and Supplier category, we have a loyal band of designers and assemblers, but we would like to be in a position to attract many more. If you are in the design community, please let us know how we can help.

**Bill Wilkie**





## ICT / NUKCG

### *Annual Foundation Course*

A recognition of changing technologies and a new emphasis of training has led us to update the syllabus to encompass the future training needs of the UK Printed Circuit Industry.

The well established formula of utilising the extensive knowledge of lecturers from supply houses and PCB producers will be extended to cover assembly shops and problem solving techniques to ensure that candidates are given a broad based training schedule on all aspects of the PCB industry.

The event will be held as usual on

### **THE LOUGHBOROUGH UNIVERSITY CAMPUS**

which has a full range of residential and tutorial facilities

**26 - 29th March 2012**

Please address all enquires to :-

[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)