

# Journal of the Institute of Circuit Technology

## 2012 Events

8th February 17.00 Registration  
**17.30 ICT Evening Seminar.**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)  
**Norfolk Arms Hotel, Arundel.**  
 supported by CCI Eurolam

Monday 19th March  
 16 MRC Event  
 Plastic & Printed Electronics:  
 Interconnects & manufacturing challenges  
 At Henry Ford College, Loughborough University  
 To register for this free event please send an e-mail to:-  
[lemrc@lb.oro.ac.uk](mailto:lemrc@lb.oro.ac.uk) before March 15th

26th March - 29th March  
**ICT/NUKCG Annual Foundation Course**  
 at **Loughborough University**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)

18th-19th April  
 National Electronics Week (NEW)  
 NEC Birmingham

12th June Tuesday  
**38th ICT Annual Symposium**  
 at **Imperial War Museum, Duxford**  
[bill.wilkie@InstCT.org](mailto:bill.wilkie@InstCT.org)

29th June Friday  
 Dissemination Seminar  
 Results from Applied Research Projects in the  
 Surface Engineering and Printed Circuit Sectors  
 by the Surface Engineering Association  
 at Federation House, 10 Vyse St., Birmingham  
[info@sea.org.uk](mailto:info@sea.org.uk)

6th September Thursday  
 20th Southern **PCB Golf Day** at the  
 "The Wiltshire Golf and Country Club".  
[rwoodroe@aol.com](mailto:rwoodroe@aol.com)

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### The Membership Secretary's notes - March 2012

With Easter just around the corner, it is time once again for the ICT/NUKCG Annual Foundation Course at Loughborough University. This course has been running since 1980, when it was founded under the auspices of the Northern UK Circuit Group. This group has now been disbanded, but the course retains the title to show and remind us of its origins. The course has changed over the last thirty two years, whilst maintaining its essential premise – that of encouraging Industry experts to deliver the presentations to delegates. Initially, the course was a two-week residential course at Borders College (part of Heriot Watt University) with a factory visit – usually Exacta or Bepi, practicals and a multi-choice examination at the end accompanied by a book prize for the top scorer.

It has been running at Loughborough University since 2005 and the first day is now hosted by Invotec Group so that we can take in facility visits of both their Tamworth facility and the Printed Electronics Manufacturing Area. We must be doing something right, because this year we have attracted our full complement of 30 delegates from 15 different companies, including 12 PCB fabricators!

When first reading the above Membership Secretary's Notes the thought occurred that we and others have spent very considerable effort organising Courses about Circuit Technology.

Way back in the 'seventies the IMF (Institute of Metal Finishing) were organising evening Courses at the London School of Printing in Basic Methods of Making Printed Circuits, and my Employers joined the IMF solely to be able to send Employees. Then there were enjoyable evening discourses by Frank HicksArnold at the Taplow Telephone Research Laboratories and Twickenham Technical College.

In the middle 'seventies John Brooks organised week long courses at The Bournemouth Technical College on behalf of the ICT , and an astonishing 35 courses between Sep.83 and Nov88 were discovered when researching the ICT courses run by Pat Kirby at Oxford University.

It would seem that between us the Institutes have more than satisfied the two most important Objectives of the Institute of Circuit Technology, namely :-

- a) To provide a forum for members of the Institute of Circuit Technology to discuss the technology of printed circuits and related technology.
- e) To hold meetings, seminars and training courses for the exchange and dissemination of knowledge and to sponsor national and international meetings for this purpose

Editor  
(Bruce Routledge)

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**Council** Martin Goosey (*Chairman*), Andy Cobley (*Deputy Chairman*), John Walker (*Secretary*), Chris Wall (*Treasurer*),  
**Members** William Wilkie (*Membership Secretary & Events*), Bruce Routledge (*the Journal*), Richard Wood-Roe (*Web Site*),  
**2011/2** Lawson Lightfoot, Tom Parker, Steve Payne, Peter Starkey, Francesca Stern, Bob Willis.

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#### Membership

New members notified by the Membership Secretary

Associate Member (A.M.Inst.C.T.)	Member (M.Inst.C.T.)
10232 Tom Bruce	10230 Graham Pemberton 10231 Roper Michael 10233 Steve Lord 10234 Bryan Lucas

#### Corrections and Clarifications

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*The Journal of the Institute of Circuit Technology is edited by Bruce Routledge on behalf of the  
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Peter Starkey  
reviews a webinar  
organised by Bob Willis  
on  
**PCB Nickel-Gold Surface Failures**

PCB Nickel-Gold Surface Failures: the Good, the Bad and the Ugly Seminar – not an ageing spaghetti western produced by Sergio Leone and starring Clint Eastwood but a state-of-the-art technical webinar on a significant industry issue, produced by Bob Willis and starring leading authorities in the field of printed circuit materials, manufacture, test and troubleshooting: Nigel White from Atotech, Dennis Price from Merlin Circuit Technology, Dr Chris Hunt from the National Physical Laboratory and Professor Martin Goosey from the Institute of Circuit Technology

**Bob Willis** put the topic into context with statistics from SMART Group web surveys indicating that, of the PCB defects reported by users, solderable finish faults accounted for more than 35% of the total. Then, with reference to IPC acceptability specifications IPC-A-600, IPC-A-610, the IPC Test Methods Manual, J-Standards and solderable surface finish standards IPC-4552, IPC-4553 and IPC-4554, he showed a series of photographs illustrating many examples of PCB assembly process problems including surface non-wetting, black tarry pads, solder finish lifting, nickel-gold tape-testing failures and BGA-package-to-PCB separation.

Willis then handed over to **Nigel White**, who gave an introduction to electroless-nickel-immersion-gold technology from the perspective of the process supplier, beginning by listing the attributes expected by the industry: multiple soldering capability for both tin-lead and lead-free processes, aluminium wire bondability, constant contact resistance for keypads and switches, planarity, a phosphorus content in the range 7-10%, and a 12-month shelf life. ENIG was a two-stage metal deposition process, where the nickel-phosphorus functioned as a diffusion barrier and added strength to plated-through holes and vias.

The solder joint was actually formed as a tin-nickel intermetallic. The thin gold layer minimized the interaction of nickel with the environment and was dissolved in the solder. ENIG was a mature process, which had been used since the early 1990s.

The reaction mechanism involved the deposition of a nickel-phosphorus on a palladium-sensitised copper surface by autocatalytic reduction, followed by the semi-autocatalytic immersion deposition of gold on the nickel surface. White described the process in detail, including some available options to

overcome problems such as the entrapment of chemistry in partially plugged via holes, and some notes on process performance and deposit characteristics.

Concerns and limitations were the cost of precious metal, the potential brittleness of the tin-nickel intermetallic, corrosion of nickel by the immersion gold solution, the tight process control required and the unsuitability of ENIG for gold wire-bonding applications. But on the positive side, ENIG was suitable for multiple lead-free soldering, it had planarity to suit surface mount component placement requirements, and the nickel barrier layer prevented dissolution of copper by solder.

It also exhibited good shelf life, good resistance to corrosive environments, presented a good surface for ICT probing and contact switching applications and was suitable for aluminium wire-bonding

Nigel White having described ENIG from the supplier side, **Dennis Price** gave a user view based on his many years of practical experience at Merlin Circuit Technology in controlling and optimising the performance of the process. He emphasised the importance of proper copper surface preparation prior to the application of solder mask: Merlin's preferred method was low-pressure pumice scrubbing with nylon-bristle brushes. Price gave a word of caution regarding solder mask adhesion failure: in the past, many fabricators had attempted to overcome major adhesion problems by initially only part-curing the solder mask to retain flexibility during ENIG processing, with apparent success but with the consequence that sulphur-containing compounds were leached out and contaminated the nickel bath.

Price went through Merlin's 23-step process sequence stage-by-stage, with hints, tips and observations, stressing the relevance and importance of meaningful laboratory analysis, data recording and statistical process control. One of the main causes of skip plating was, as Nigel White had commented, entrapment of micro-etch solution in partially-closed via holes, which could bleed out and poison the palladium

activator on local features. Extraneous nickel deposits could result from wicking of activator into the cut ends of glass yarns in non-plated holes or the activation of trace residues of un-etched copper metal in the laminate surface. Although it could appear attractive to run electroless nickel baths for many metal turnovers to reduce process costs, it had been shown that the increased concentration of contaminants and by-products could result in nickel deposits which were more prone to surface hyper-corrosion during the plating of immersion gold. Price also underlined the importance of topping-up of evaporation losses by little-and-often additions, and advocated the use of an automatic controller for the electroless nickel plating bath, which could continuously monitor nickel concentration and made additions of nickel and hypophosphite replenishers in small increments to maintain the chemistry within close working limits with a minimum of operator dependence.

After the comprehensive chemistry lessons came a presentation on PCB failure analysis techniques from **Chris Hunt**, who described how defects were identified and failure mechanisms studied and interpreted, using the wide range of test and inspection techniques available at NPL, including optical, x-ray and scanning electron microscope examination, micro sectioning, x-ray fluorescence spectroscopy, shear testing and hot pull testing, illustrated with many examples. He gave details of the Defect Database on printed board assembly and material issues, managed by the NPL Electronics Interconnection Group as a service to the electronics industry. Any visitor to the database could add defect information and photographs from his own observations, and have free access to the continuously increasing catalogue of reference data and images to assist in implementing corrective actions in processes or designs.

Next to speak was **Martin Goosey**, who was coordinating a three year EC Framework 7 project known as ASPIS - Advanced Surface Protection for Improved Reliability PCB Systems. The ASPIS project aimed to develop new, more reliable materials, processes and testing procedures in order to address the key issues associated with ENIG finishes. The project had adopted a number of technical approaches ranging from an in-depth study of the fundamental mechanisms that influence the metal deposition and subsequent reliability, to the development of new chemical processes based on both traditional aqueous chemistry and new ionic liquids. In addition, work was being carried out to develop better methods for identifying failure

mechanisms and a non-destructive prognostic screening tool that could be used to give warning of latent problems on printed circuit boards in advance of components being soldered on to them. Progress to date included the demonstration of nickel and gold deposition from novel ionic liquid-based chemistries, and a more detailed understanding of the key factors influencing the formation of "black pad" defects.

**Bob Willis** gave the final presentation "BGA Joint Inspection Using Dye & Pry Testing – How to Do It Yourself". The dye-and-pry technique was useful as a means of detecting subtle open circuits caused by wetting problems on pad surfaces or flexing of the BGA or the PCB during reflow. On ENIG-finish PCBs, as the solder paste fused it would dissolve the gold and apparently wet the pad, but could still fail to form a sound intermetallic bond to the nickel, and this type of defect was very difficult to detect by traditional methods of optical or x-ray inspection or electrical test. Dye penetrants had been used for many years in the testing of welded joints and castings prior to destructive analysis, and Willis explained how they could be used as the basis of a low-cost alternative test to quickly and straightforwardly reveal the location of a failure in a BGA assembly. In practical terms, the procedure was to impregnate the suspect area with a proprietary dye, using vacuum assistance if possible, dry it in an oven then pry off the component with a chisel and examine the remains of the joints for evidence of dye penetration. As usual, he provided an abundance of pictorial illustrations, and explained in detail how to interpret and record the results.

*The Good, the Bad and the Ugly Seminar proved to be an informative and educational event. Three hours is a long time to hold peoples' attention but Bob Willis did a very professional job of maintaining the continuity of the programme and moderating the real-time question-and-answer session, which generated some highly interactive dialogue and exchange of ideas and experiences.*

**Pete Starkey** F.Inst.C.T.  
Technical Editor  
I-Connect007

*"Editors note: The webinar presentations can still be viewed by members at:-*

*[www.instct.org/seminar-reports](http://www.instct.org/seminar-reports)"*



# Graphene and its Potential Interconnect Applications

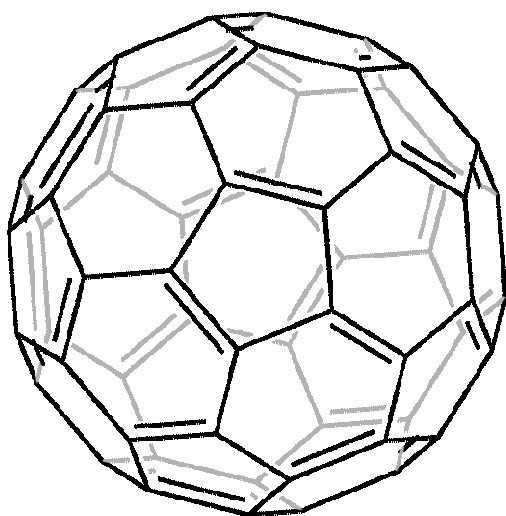
Martin Goosey – ICT Chairman



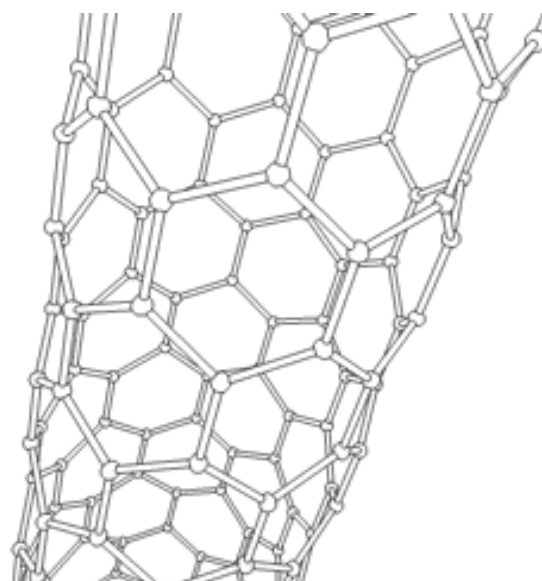
Over the last twenty years or so there has been increasing interest in the field of nanotechnology, which is essentially concerned with materials having dimensions below 100 nm. There is a wide range of materials that can be produced with nanoscale dimensions and these often exhibit interesting properties that differ markedly from those found in the equivalent bulk materials.

One such group of materials are the fullerenes, which is the name given to any molecule composed entirely of carbon and in the form of a hollow sphere, ellipsoid or tube. Spherical fullerenes are often known as buckyballs, and they are the same shape as some designs of footballs. These were first synthesised in 1985 and, since then, there has been a huge amount of research and interest in buckyballs and related fullerenes. Cylindrical fullerenes soon followed buckyballs and these were first synthesised in 1991. These are commonly called carbon nanotubes (CNTs). They can be of the single walled or multiwalled variety and, in addition to their very high strengths, they have been found to possess unique electrical and thermal conductivities.

The structure of a buckyball is shown below, and top of RH column is an example of a single walled CNT.

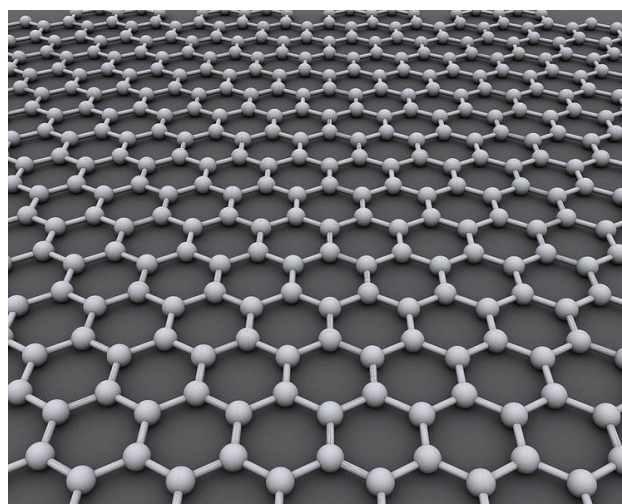


**Buckyball**



**Single walled CNT**

If one imagines opening up the carbon nanotube structure above, it would form a single atom thick sheet of carbon with a honeycomb structure similar in appearance, but on a much smaller scale, to 'chicken wire'. This is essentially the structure of graphene, which can more accurately be described as an allotrope of carbon whose structure is a one atom thick planar sheet of densely packed carbon atoms in a honeycomb crystal lattice.



**The single carbon layer structure of graphene**

## The single carbon layer structure of graphene

The more common and well known material graphite is made up of many layers of graphene stacked on top of each other. The structure of graphite has been known for a long time, but it was only in 2004 that individual graphene planes were isolated. This initial isolation was achieved using a laborious method involving adhesive tape, but a number of other more efficient methods have subsequently been developed. These include the use of established chemical vapour deposition techniques and more recently, by burning magnesium in dry ice (1).

As a result, graphene has become much more widely available, which in turn has enabled the material to become the focus of a huge international research activity (2).

The very interesting electrical properties of carbon-based nanomaterials such as graphene have been known for some time and, as a result, much of the recent research has been focussed on potential electronics related applications. Some of the key properties of graphene that make it of such interest for use in electronics are its very high electrical conductivity, high carrier mobility and optical transparency. Graphene also has a higher thermal conductivity than any other known material. One particular potential application area of interest is in the use of graphene as a replacement for indium tin oxide (ITO) in transparent electrodes.

Indium is becoming increasingly scarce and, as a consequence, its price is increasing. There is thus a growing demand for alternative transparent conducting materials. Graphene has the potential to enable transparent electrodes to be made with higher transparency than ITO while, at the same time, being more electrically conductive. It could also be much cheaper than conventional transparent conductors so, in the future, graphene may offer a viable alternative to ITO in a wide range of display applications.

There is also increasing interest in the development of energy storage devices that can be recharged relatively quickly, compared to conventional batteries, for use in electric/hybrid vehicles and related applications. One route for achieving this is via the use of

so called ultra-capacitors. These are electrochemical capacitors that offer significantly higher energy densities than conventional capacitors.

The surface area of a single graphene sheet can be much greater than materials such as the activated carbons currently used in electrochemical double layer capacitors. Graphene has thus been evaluated as a new carbon-based material for storing electrical charge in ultra-capacitors (3, 4). The reported results have typically been very positive and suggest that graphene has significant potential for use in high performance electrical energy storage devices.

For the longer term, researchers are hoping to be able use graphene to fabricate advanced semiconductor devices and it is, for example, being investigated as a potential alternative to the materials such as gallium arsenide that are used in high-frequency communications applications. Discrete graphene transistors were first fabricated a while ago and, in June 2011, researchers at IBM announced that they had designed high speed circuitry using several layers of graphene deposited onto a silicon wafer (5). However, it should be noted that graphene does not have the same physical properties as conventional semiconducting materials. For example, the material does not have a band gap and so it cannot be used to completely switch on and off in the same way as conventional transistors.

More recently, and perhaps even more interestingly, it has been reported that Korean researchers based at the country's Soongsil University in Seoul and Sungkyunkwan University in Suwon have produced stretchable graphene transistors (6). The researchers fabricated a stretchable, transparent graphene-based transistor and found that, due to graphene's excellent optical, mechanical and electrical properties, the transistor overcame some of the problems faced by transistors made of conventional semiconductor materials. For example, the devices exhibited stable operation when stretched up to 5%, even after more than 1000 cycles.

This development may open up a wide range of potential new applications based on stretchable

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- 2) *Graphene: Status and Prospects.*  
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pp 9-13, (Jan. 2008).
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Jong-Hyun Ahn.  
*Nano Letters*, 11, (11), pp  
4642-4646, (2011).

electronics, such as wearable displays, conformal sensors and rollable displays.

Stretchable transparent graphene interconnects have also been used with arrays of microscale inorganic light emitting diodes on rubber substrates.

In a paper published by Rak-Hwan Kim et al (7), the authors describe the fabrication and design principles for using transparent graphene interconnects in stretchable arrays. In particular they demonstrated some of the advantages of using graphene for this purpose, including its ability to conform to surface topography, thereby enabling contacts to be produced even in deeply recessed areas. The paper clearly demonstrates that graphene interconnects offer attractive properties for use with LEDs in a range of applications.

Graphene has also been used to produce three dimensional stacked multilayer interconnects (8) although it appears that the overall intrinsic resistivity tends to decrease with increasing number of layers.

It is also interesting to consider whether graphene may have any direct applications as an interconnect material at both the printed circuit and semiconductor levels. With the growing interest in printed and plastic electronics, there is a need for highly conductive inks that can be used to deposit conductors onto a variety of substrates. Graphene would thus appear to be an ideal component for use in these inks and there is already a commercially available product from a US company called Vorbeck Materials (9) known as Vor-ink. In this type of application graphene not only offers excellent conductivity but also a lower cost than the silver traditionally used in conductive inks. Another advantage for some applications is that the printed materials can be wrinkled or crumpled without adversely impacting the functionality.

In the case of the much finer interconnects required with semiconductor devices, it seems that graphene may provide a viable alternative to conventional interconnect metals such as copper. Interconnects in these types of semiconductor applications will soon be in the region of a few tens of nanometres and, on this scale, the increased resistivity of metals such as copper means that it is likely to have a detrimental impact on future device performance i.e. operating speed. As semiconductor

interconnect dimensions move further towards the low nanometre-scale region, the grain size of copper becomes an increasingly important factor in determining conductivity, which is affected by scattering at the grain boundaries and at the side walls. Researchers at the Georgia Institute of Technology's Microelectronics Research Center have demonstrated the potential for graphene to replace copper interconnects in future integrated circuits (10). In this work, graphene interconnects were fabricated and their resistivities compared to that of copper. It was found that the average resistivities at line widths between 18 nm and 52 nm were about three times that of an equivalent copper wire, while the best resistivity was similar to that of copper.

In spite of the promising predictions about the excellent current-carrying capability of graphene, actual demonstration and characterisation of the properties and performance in real interconnect applications had, until the last couple of years, been relatively limited. However, more recently, a paper published by Xiangyu Chen of Stanford University and co-workers from Toshiba and MIT described the first monolithic integration of graphene with commercial CMOS technology and the first experimental demonstration of on-chip graphene interconnects that operated above 1 GHz (11). Also, researchers at the University of Cambridge's Department of Engineering have also recently reported the use of graphene in the fabrication of thin film transistors (12). The team, lead by Andrea Ferrari, produced a graphene-based ink by the liquid phase exfoliation of graphite in N-methylpyrrolidone. The ink was then used to print thin-film transistors, with mobilities of up to

$$\sim 95 \text{ cm}^2\text{V}^{-1}\text{s}^{-1},$$

as well as transparent and conductive patterns with

$$\sim 80\% \text{ transmittance and}$$

$$\sim 30 \text{ k}\Omega/\text{square}.$$

This work could thus provide a new processing route for producing all-printed, flexible and transparent graphene devices on a wide range of substrates.

**7)** *Stretchable, Transparent Graphene Interconnects for Arrays of Microscale Inorganic Light Emitting Diodes on Rubber Substrates.*

Kim R. H., Bae M. H.,  
Kim D. G., Cheng H.,  
Kim B. H., Kim D. H.,  
Li M., Wu J.,  
Du F., Kim H. S.,  
Kim S., Estrada D.,  
Hong S. W., Huang Y.,  
Pop E. and Rogers J.

*American Chemical Society, Nano Letters, 11 (9), pp 3881-3886, (2011).*

**8)** *Three-Dimensional Stacked Multilayer Graphene Interconnects.*

Yu T.,  
Chen-Wei Liang C.  
W., Kim C.,  
Song E. S. And  
Yu B., IEEE

*Electron Device Letters, Vol.32, Iss. 8, pp 1110-1112, (August 2011), ISSN: 0741-3106.*

**9)** see [www.vorbeck.com](http://www.vorbeck.com) (accessed 12th January 2012)

**10)** *Resistivity of Graphene Nanoribbon Interconnects.*

Murali R.,  
Brenner K.,  
Yang Y.,  
Beck T. And  
Meindl J. D.,

*Electron Device Letters, IEEE, Volume 30, Issue 6, pp 611-613, (June 2009), ISSN: 0741-3106.*

**11)** *Experimental Demonstration and Characterization of on-chip high speed graphene interconnects.*

Chen X.,  
Akinwande D.,  
Lee K. J.,  
Close G.,  
Yasuda S. and Paul B.,

*Bulletin of the American Physical Society, APS March Meeting 2010, Volume 55, Number 2, (2010).*

**12)** *Ink-Jet Printed Graphene Electronics.*

Torrisi F., Hasan T.,  
Wu W., Sun Z.,  
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W., Jung S. J.,  
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Ferrari A. C.,

*arXiv:1111.4970v1 (cond-mat.mtrl-sci), (21 Nov 2011.)*

With its better electrical resistivity on this scale, as well higher electron mobility, higher thermal conductivity, greater mechanical strength and reduced capacitance coupling between adjacent wires, graphene could be a promising material for replacing conventional metal interconnects on the nanometre scale. Also, graphene can be patterned using conventional microelectronics processes, so it might be possible to transition from copper without the need for any new manufacturing techniques.

Such is the level of interest in graphene and its future potential that even the UK government appears to be willing to support efforts to bring about the commercialisation of this very interesting novel material. A statement on the Conservative Party website (13) recently said; "We will invest £50 million in a Graphene Global Research and Technology Hub to commercialise graphene. This will capitalise on the UK's international leadership in the

field. It will act as a catalyst to spawn new businesses, attract global companies and translate the value of scientific discovery into wealth and job creation for the UK".

Graphene is clearly a very interesting new material with a range of properties that are often superior to more familiar and established materials. As experience of producing and processing graphene grows, it seems fairly certain that it will be increasingly used in a wide range of electronics manufacturing applications. Despite the fact that it is a very different material from those with which the electronics industry is more familiar, and that it has a number of limitations, graphene is likely to be a key new material that will enable continued evolution in conventional electronics and also provide a solution for new applications that are currently hampered by materials limitations.

Prof. Martin Goosey  
ICT Chairman

#### References 13) see

[www.conservatives.com/News/News\\_stories/2011/10/Osborne\\_together\\_we\\_will\\_ride\\_out\\_the\\_storm.aspx](http://www.conservatives.com/News/News_stories/2011/10/Osborne_together_we_will_ride_out_the_storm.aspx)  
(accessed 12th January 2012).





**Peter Starkey**  
reviews **le MRC Event**  
Plastic & Printed Electronics:  
interconnects & manufacturing challenges

With research, development and commercialisation activity in plastic and printed electronics continuing to gather momentum, it was appropriate that the Innovative Electronics Manufacturing Research Centre (leMRC), who support an extensive portfolio of projects in this technology area, should organise a dedicated seminar at their base in Loughborough University in the East Midlands of the UK.

producing hundreds of thousands of units per annum of plastic logic displays based on E-ink with an all-plastic backplane technology. Joimel related some of the challenges encountered in developing a volume-capable process and how they had been overcome, beginning with equipment differences, process specifications, materials characterisation and production control, then aspects of training and know-how for a new team whose background was mainly in silicon semiconductor manufacture. He discussed manufacturability from the point of view of achieving consistency and repeatability, with reference to material analysis and measurement techniques, quality, reliability and lifetime behaviour issues, and yield enhancement strategies.

As an example of a commercial product currently in stable volume production, Joimel described the characteristics of the Plastic Logic 100, a lightweight large-format electronic textbook designed for the education sector, with the significant benefit that the display was all-plastic and therefore shatterproof. Future application areas included interactive signage, phone displays, smart cards and sensors.



**Dr Darren Cadman**

leMRC Research  
Co-ordinator

**Dr Darren Cadman** welcomed delegates, gave a brief overview of the aims and objectives of leMRC and introduced a comprehensive and well-balanced programme of presentations addressing the manufacturing challenges of printed and plastic electronics.



**Professor Martin Taylor**

Bangor University



**Jerome Joimel**

Plastic Logic Ltd

Keynote speaker for the morning session was **Jerome Joimel** from Plastic Logic Ltd, with a paper entitled "Developing a high volume manufacturing process using plastic electronics – challenges on the way from lab to fab"

Plastic Logic, originally a Cambridge University spin-off, had established a manufacturing facility in Dresden, Germany, in 2008 which had been in full production since 2010 and was presently

**Professor Martin Taylor** of Bangor University gave a fascinating presentation on "Printed electronics: Device production, characterisation & simulation", first describing the roll-to-roll vacuum deposition process developed at University of Oxford, which was capable of producing reliable working thin-film transistors by evaporation and in-situ e-beam polymerisation of diacrylate monomer on to a 75 micron polyester substrate followed by evaporation of a pentacene layer. Good results had also been observed with pentacene and dinaphthothieno thiophene thin-

film transistors on polyethylene naphthalate substrates.

Current work at Bangor focused on characterisation and simulation of a range of thin-film transistors, capacitors and inverters of different geometries and aspect ratios, using UTMOST-4 modelling software. Although some of the semiconductor theory may have been beyond the comprehension of many in the audience, Professor Taylor explained clearly how key parameters could be extracted, and commented on the success of early exercises in circuit simulation.



**Martin Wickham**

National Physical Laboratory

**Martin Wickham** from the National Physical Laboratory gave the first public-domain report on the progress of a collaborative project named **ReUSE: Reusable, Unzippable Sustainable Electronics**, an innovative enabling technology for the fabrication of sustainable multi-layer electronics assemblies. He set the scene with some remarkable statistics concerning printed circuit waste in the UK. It had been estimated that about 85% of scrap PCB assemblies ended up in landfill, of which 70% was non-metallic content amounting to around 1 million tonnes annually, and that WEEE – waste from electrical and electronic equipment – was growing three times faster than other waste streams. Typically, only high pin-count socketed devices were physically removed from electronic assemblies, the rest of the assembly being shredded for precious metal reclamation and subsequent disposal to landfill.

The aim of the ReUSE project was to develop an interconnection technology based on special polymer layers and binders designed to allow straightforward, end-of-life disassembly with easy reuse and recycling. A series of technology demonstrators had been constructed and Wickham took as example an inverter assembly for an electroluminescent lamp. This consisted of a thin flexible circuit assembled with standard tin-finished components by normal SMT techniques using an isotropic conductive adhesive and bonded to a rigid base. The assembly had been extensively tested for reliability and proved to be fit-for-purpose. However, Wickham showed that at nominal end-of-life a simple immersion in hot water allowed the assembly to be “unzipped” – the

components to be removed without damage to leads or terminations and the flex circuit to be removed from the rigid base. He believed that recovery levels in typical assemblies would be improved to at least 90%, and that the ReUSE technology would lend itself readily to rigid, flexible and 3D structures.



**Dr David Hutt**

Loughborough University

Conductive inks and adhesives are key materials in plastic and printed electronics technologies, and the majority rely on silver as the conducting element. **Dr David Hutt** from Loughborough University reviewed developments in the use of copper as a more abundant and lower-cost alternative to silver, and also explored the feasibility of combining the operations of forming conductors and assembling components.

A fundamental difference in the nature of copper compared with silver was that its oxide was non-conductive, so the principal initial challenge was to produce an oxide-free copper powder and to preserve the surface against further oxidation. This had been achieved by treating de-oxidised copper powder with a process that coated each particle with a self-assembled organic monolayer, which enabled it to be stored for several weeks in a freezer. Conductive pastes had been formulated using 10 micron powder with one-part and two-part epoxy resins at 85.7% by weight metal loading. These had been stencil printed on glass and cured at 150°C in an inert atmosphere, with conductivity comparable to typical air-cured silver-loaded resin. The copper-loaded material did not give good results if cured in air. Best results were obtained with the one-part epoxy formulation. Inert-atmosphere microwave curing was an alternative which gave good conductivity in a shorter cycle time. Conductor resistance had been observed to increase during reliability testing in 85°C / 85%RH damp heat conditions, but conformal coating overcame this effect. Dr Hutt showed examples of functional circuits which had been successfully produced in a combined circuit formation and component interconnection operation.

The UK government recognised the significance of “plastic electronics” – a term encompassing all classes of printed and organic electronics – as a sector in which Britain had potential for leadership in research, development



**Chris Williams**

Logystyx UK Ltd

and manufacturing, creating opportunities for employment and economic growth, and had published a guide to promote the UK's capabilities, designed to be used by commercial and academic groups, within the UK and overseas, looking for development partners or suppliers. A new edition of the guide was shortly to be published by the Department of Business, Innovation and Skills: The BIS Guide to Capability: Plastic Electronics in the UK 2012. **Chris Williams** of Logystyx UK Ltd was engaged in the compilation of data for the guide, and explained that any organization in the UK involved in plastic electronics was entitled to a free entry, provided their details were supplied before the deadline of **31st March 2012**.



**Dr Steve Jones**

Printed  
Electronics Ltd

**Dr Steve Jones** of Printed Electronics Ltd admitted that he was out of his comfort zone – Professor Martin Goosey had asked him to deliver the afternoon keynote from a “philosophical”, rather than his usual technical, point of view. And he gave an inspirational presentation: smooth, professional and well-researched, on a theme of invention and innovation, as he described some of the obstacles to be overcome in taking printed interconnects from R&D to commercialisation.

Defining “invention” as the creation of a novel idea, and “innovation” as the commercialisation of novel ideas, he explored the flow from discovery, through engineered product to societal benefit, remarking that since the 1970s and 1980s, not much had happened in the way of true innovation; the **21st** century was characterised by incremental improvements. “Radical or transformational innovation produces substantial improvements, radically alters or even creates markets. Printed electronics sits here!”

Reviewing the decline of manufacturing in the UK, and the risk-averse cultural resistance to change of the few remaining “big companies”, Dr Jones discussed the attitude of governments past and present, and how manufacturing had finally been recognised again as a fundamentally important area to be helped and encouraged, with the Technology Strategy Board and Research Councils supporting technology, sector and cluster development.

Digitisation and modularity had made it possible to separate R&D and design from production. Few vertically-integrated companies remained and global technology brands had shown that manufacturing could be outsourced and off-shored without damaging their ability to innovate. “Who makes electronics?” he asked: “EMS and ODM companies. And how can printed electronics compete with them?” He believed that the UK was well placed from a technology standpoint. The TSB and academic institutions had been supportive and it was acknowledged that the UK and Germany were leaders in the field of printed electronics.

Whilst acknowledging the need to be heroic and passionate and to explore boundaries, Dr Jones hoped to avoid being remembered for having died heroically or being found lying face-down in the desert with an arrow in his back! Collaboration and co-operation were what was important for small companies and he referred to the business strategy of his own company, which was involved in many collaborative ventures and for which EMS and ODM offered opportunities to develop products in the short term. The potential for printed electronics was huge: not just to replace conventional electronics but to transform where electronics could go.



**Dr Paul Reip**

Intrinsic  
Materials Ltd

Back to the technical agenda, it was the turn of **Dr Paul Reip** of Intrinsic Materials Ltd to give an update on developments in nanoscale metal inks for printed electronics. Intrinsic Materials had spun out of Qinetiq, the British global defence technology company, formerly the UK government Defence Evaluation and Research Agency and its particular expertise was the ability to manufacture nanoparticles, with over 20 years of experience in



nano-copper: understanding the product and being able to produce it repeatably.

David Hutt had earlier discussed applications of copper as an alternative to silver in the context of micron-particle formulations for stencil-printing; Dr Reip looked at a parallel scenario using nano-copper as a silver alternative in ink-jet formulations.

Again the primary obstacle to be overcome was the tendency of copper to oxidise, greatly accentuated at nano-particle sizes. Intrinsic had developed a proprietary organic coating, typically 1 nanometre thick on 35 nanometre particles, which inhibited oxidation. Jettable ink formulations had been validated on both XAAR and Dimatix print-heads and successfully printed on multiple substrates. Photonic curing techniques had been employed, using pulsed UV or laser, to cure the ink in milliseconds with no substrate damage, which offered opportunities for high-speed roll-to-roll processing.

In response to market demand, screen printable versions had been formulated which had bulk resistivity values approaching that of pure copper, at between one third and one fifth the price of equivalent silver-based inks. Besides nano-copper inks, Intrinsic had developed jettable nickel and silicon products, with applications in displays, smart media and photovoltaics.



**David Watson**

Heriot-Watt University

**David Watson** from Heriot-Watt University described a process for laser direct writing of metals on plastic substrates, with particular reference to nano-silver on PMDA-ODA polyimide film, which could achieve line widths of 10 microns and less.

The silver-on-polyimide process involved six steps, the first of which was hydrolysis of the polyimide surface with potassium hydroxide, followed by immersion in silver nitrate solution to replace potassium ions with silver ions. In the next stage, a solution of methoxy polyethylene glycol was sprayed on the surface and dried. This functioned as a kind of photosensitiser by acting as an electron donor to reduce silver ions to nano-silver particles when subsequently imaged by selective exposure with a UV laser. After exposure, unexposed silver ions were removed and the surface was re-oxidised by immersion in dilute sulphuric acid and the work was annealed to coalesce the silver particles into a form suitable to act as a seed layer for subsequent deposition of

silver from a proprietary electroless plating bath.

Current investigations were directed at the characterisation of a range of proprietary polyimide films, and the optimisation of the laser exposure and annealing conditions.

A potential "green" alternative to methoxy polyethylene glycol as a photo-reducing agent was natural chlorophyll, extracted from spinach and sensitive to blue visible light rather than UV, resulting in less substrate degradation.



**Dr Steve Wakeham**

Plasma Quest Ltd

The concluding paper came from **Dr Steve Wakeham** of Plasma Quest Ltd., and was entitled: "HiTUS – an enabling technology for the plastic electronics industry." HiTUS was a technique for sputtering thin films, which differed from traditional ion-beam-source and magnetron deposition systems by generating a remote plasma in a side arm adjacent to the deposition chamber. Ions generated from this plasma system had low energy and required the application of a bias on the target, enabling a high degree of control on the deposition variables. Key advantages of the system were that it operated at low temperature and was therefore compatible with plastics, and that it offered high deposition rates with controllable stress, increased adhesion and increased densification. It was capable of depositing low-stress, fully-densified ultra-thin coatings on to temperature-sensitive plastics. Some examples were ultra-thin gold on PET, PEN and BOPP films, dielectric mirrors on PEN, multilayer colour filters on PEN consisting of 19 to 25 alternate layers of silica and hafnia, and the fabrication of photoluminescent and electroluminescent devices and plastic-compatible thin-film transistors.

In his closing remarks, leMRC Industrial Director Professor Martin Goosey commented that although plastic and printed electronics were unlikely to replace silicon, there were many applications where they potentially offered innovative performance together with low-cost manufacturability.

leMRC have established a reputation for organising and managing technical conferences and seminars of the highest calibre, and the team are to be commended for yet another outstanding event.

**Pete Starkey** F.Inst.C.T.

Technical Editor

I-Connect007



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## The Membership Secretary's notes - March 2012

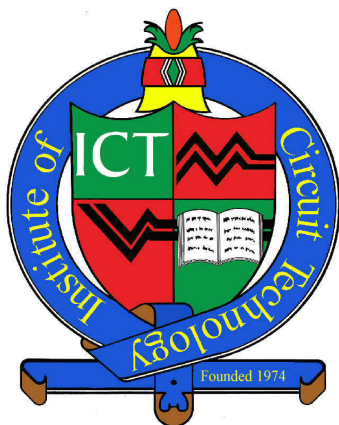


With Easter just around the corner, it is time once again for the ICT/NUKCG Annual Foundation Course at Loughborough University. This course has been running since 1980, when it was founded under the auspices of the Northern UK Circuit Group. This group has now been disbanded, but the course retains the title to show and remind us of its origins. The course has changed over the last thirty two years, whilst maintaining its essential premise – that of encouraging Industry experts to deliver the presentations to delegates. Initially, the course was a two-week residential course at Borders College (part of Heriot Watt University) with a factory visit – usually Exacta or Bepi, practicals and a multi-choice examination at the end accompanied by a book prize for the top scorer.

It has been running at Loughborough University since 2005 and the first day is now hosted by Invotec Group so that we can take in facility visits of both their Tamworth facility and the Printed Electronics Manufacturing Area.

We must be doing something right, because this year we have attracted our full complement of 30 delegates from 15 different companies, including 12 PCB fabricators!

*Bill Wilkie*



## 38th Annual Symposium of The Institute of Circuit Technology

# Manufacture and Materials

Tuesday 12th June 2012

at the Imperial War Museum, Duxford

### Agenda

09.50 Opening Address **Bill Burr** - *Bpa Consulting*

'Metal-in-Board' **Bill Burr** - *Bpa Consulting*

I Imaging Equipment **Jake Kelly** - *Viking Test*

ASPIS project **Prof. Martin Goosey** - *ICT Chairman; Director IeMRC*

Printing, Coating  
and Hot Embossing **Thomas Kolbusch** - *Coatema*

12.30 - 13.30 **LUNCH and TABLETOP EXHIBITION**

Imaging Equipment **Lawson Lightfoot** - *Rainbow Technology Systems Ltd.*

Material Innovations  
for Power Electronics **Manfred Walchshofer** - *Panasonic*

Lean and Benchmarking  
- a Driver for Growth **Mark Knowlton** - *KPS*

15.15 **Close of Symposium**

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*The Symposium is supported by the Lamar Group*

Register for the Symposium with Bill Wilkie at

[bill.wilkie@instCT.org](mailto:bill.wilkie@instCT.org) or 01573 226 131

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