

Journal of the Institute of Circuit Technology

Vol.8 No.1Sup Winter 2015 Issue

Special issue to cover the **leMRC** and **EIPC** Conferences

2014 Events

5th June *Thursday* ICT Annual Symposium at Great Western Railway STEAM Museum, Swindon bill.wilkie@InstCT.org

23th September ICT Evening Seminar *Tuesday* at Newton House Hotel, Hayling Island <u>bill.wilkie@InstCT.org</u>

18th November ICT Darlington Evening Seminar *Tuesday* at St George Hotel, Durham Tees Valley Airport, DL2 1RH 01325 332631 bill.wilkie@InstCT.org

2015 Events

		3rd March <i>Tuesday</i>	ICT Northern Seminar and AGM at Chimney House Hotel, Sandbach
Editorial	2		www.instct.org
Council Members	2		DIII.WIIKIE@ITIStCT.org
Membership News	2	13th -16th April	ICT Annual Foundation Course
leMRC 9th Annual Conference Peter Starkey	3-8	Tuesday - Friday	at Loughborough University bill.wilkie@InstCT.org
EIPC Winter ConferenceDay 1Peter Starkey	9-13	3rd June <i>Wednesday</i>	ICT Annual Symposium at Black Country Museum
EIPC Winter ConferenceDay 2Peter Starkey	14-19	,	bill.wilkie@InstCT.org
ICT Corporate Members	20		

The Journal of the Institute of Circuit Technology Vol.8 No.1Sup

This Supplementary Issue of *The Journal* has been produced and published while the **EIPC Winter Conference** and the **9th** and final **Annual Conference of the Innovative Electronics Manufacturing Research Centre (IeMRC)** were still topical and prominent in Members minds.

Some very pertinent and interesting subjects and objects are reviewed in the following pages.

Members are urged to study the Reviews in detail, and to follow up items in which they have a particular interest with the relevant authors, initially through the professional bodies at either of the following addresses :-

EIPC - <u>www.eipc.org</u>

leMRC - <u>www.iemrc.org</u>.

Bruce Routledge Editor

Council Members 2015	 Andy Cobley (<i>Chairman</i>), Steve Payne (<i>Deputy Chairman</i>), John Walker (<i>Secretary</i>), Chris Wall (<i>Treasurer</i>), William Wilkie (<i>Membership Secretary & Events</i>), Bruce Routledge (<i>the Journal</i>), Richard Wood-Roe (<i>Web Site</i>), Martin Goosey, Maurice Hubert, Lawson Lightfoot, Peter Starkey, Francesca Stern, Bob Willis. 					
Membership		Corrections and Clarifications				
New r	nember notified by the Membership Secretary					
1034	6 Lynn Houghton F.Inst.C.T.					
		It is the policy of the Journal to correct errors in the next issue. Please send corrections to : - <u>brucer@john-lewis.com</u>				

The Journal of the Institute of Circuit Technology is edited by Bruce Routledge on behalf of the Institute of Circuit Technology. 4 Burnhams Field, Weston Turville, HP22 5AF. Tel:01296 394 383 E-mail : brucer@john-lewis.com

The Journal of the Institute of Circuit Technology Vol.8 No.1Sup March 2015

IeMRC 9th Annual Conference, 17th February 2015, Loughborough, UK

by Peter Starkey F.Inst.C,T,

There was a combination of celebration and nostalgia at the 9th and final Annual Conference of the Innovative Electronics Manufacturing Research Centre (IeMRC) at Loughborough University, UK.

Professor Paul Conway welcomed a full-house audience and reflected upon the 10-year history of the leMRC, from its origins as one of the Manufacturing Research Centres set up and supported by the Engineering and Physical Sciences Research Council (EPSRC), with the vision of being the UK's internationally recognised provider of world-class electronics manufacturing research, focused on sustaining and growing high value manufacturing in the UK by delivering innovative and exploitable new technologies and providing strategic value to the electronics industry.

It was a distinctive characteristic of the IeMRC that it had operated as a distributed operation rather than as a fixed location for its research activities. During its existence, it had funded 54 projects in 26 universities and supported the work of 162 researchers and 33 PhD students.

The Annual Conference had provided a forum for the leMRC community and industry to demonstrate and report the research being undertaken, and to form new research collaborations by promoting interaction and cooperation between academic institutions and industry. This year's event showcased the outputs of a selection of current projects with a programme of nine presentations, beginning with a keynote from **Dr Luigi Occhipinti**, National Outreach Manager for the EPSRC Centre for Large-Area Electronics, based at the **University of Cambridge**,

Dr Occhipinti explained that the EPSRC Centre for Large-Area Electronics was a partnership between Cambridge Innovation and Knowledge Centre, the Centre for Plastic Electronics at Imperial College, the Welsh Centre for Printing and Coating at Swansea University and the Organic Materials Innovation Centre at the University of Manchester, created to work with industry to address key research challenges for manufacturing large-area electronic systems, and to bridge the gap between academic research and commercial exploitation.

Large-Area Electronics included printable, flexible and organic electronics, and referred to a new way of making electronics using novel electronic materials, often formulated as inks, and low-temperature processes such as printing and coating. This approach offered the benefits of lower-cost manufacturing of systems in high volume, with new form factors and features, using technologies based on the processing of conductive polymers and nanocomposites and fabrication of devices with conductive, transparent, optoelectronic, energy harvesting, energy storage and electromechanical functionalities.

Examples included photovoltaics, lighting, displays, sensing systems and intelligent objects.

An exercise in acronyms He described high-growth emerging sectors which offered opportunities for applications of AMOLED (activematrix organic light-emitting diode) displays with OLED (organic lightemitting diode) backplanes, OPV (organic photovoltaics) for off-grid and BIPV (building-integrated photovoltaic) panels. Sensors was another area: OPD (organic photodetector) surfaces combined with OTFT (organic thin-

Large-Area Electronics



Dr Luigi Occhipinti

Devices with conductive, transparent, optoelectronic, energy harvesting, energy storage and electromechanical functionalities."



Dr Tina Lekakou

film transistors) to produce AMOPD (active-matrix organic photodetector) devices. He followed with a programme overview of some current projects, including iPESS - the integration of printed electronics with silicon for smart sensors, with an emphasis on gas sensors based on OFETs (organic field-effect transistors), FlexiPower, using printed components for RF energy-harvesting systems, and A-LITH (adhesion lithography) - for creating asymmetric nano-gaps on arbitrary substrates, amongst many others. The overall theme was the development of innovative approaches to the multi-functional system manufacture of large-area electronics using processes that minimised cost whilst optimising yield and performance

The presentation of **Dr Tina Lekakou** from **University of Surrey** certainly carried the longest title of the day: "Processing of conductive polymers and nanocomposites and fabrication of devices with conductive, transparent, optoelectronic, energy harvesting, energy storage and electromechanical functionalities."

Her initial focus was on the process modelling and optimisation of inkjet printing systems as an alternative to spin coating for the formation of transparent, electrically conductive coatings using PEDOT:PSS (poly[3,4-ethylenedioxythiophene]-poly[styrenesulfonate]). Spin coating resulted in large differences in in-plane and out-of-plane conductivity because of its effect on grain orientation. The difference was minimised when inkjet was used and the out-of-plane conductivity had been measures as 600 times higher than that of spin coated films. This gave substantial performance benefits in plastic LEDs and photovoltaics.

A parallel project had studied the fabrication of MWCNT (multi-wall carbon nanotube) coatings by spin coating, inkjet printing and electrospinning, with the objective of maximising electrical conductivity.

The application of an electrophoretic field improved transverse orientation.

The effects of dispersion techniques, solvent addition and polymer wrapping had also been investigated. Nanocomposites of MWCNTs and epoxy resin possessed very high dielectric constants, and applications in capacitors and supercapacitors were being developed.

Actuators suitable for optical applications in electronic displays had been fabricated from nanocomposites of MWCNTs and polyurethanes.

Dr Darren Southee had been experimenting with printed power sources since his days at Brunel University. He was currently working with Professor Upul Wijayantha at **Loughborough University** on broadening the integration of printed power sources with electronic systems.

They gave a joint presentation on rechargeable printed power sources. They had set out to determine the feasibility of making rechargeable energy storage devices using mass-produced printed electrodes, and to produce a demonstrator, having characterised the original electrodes produced by offset lithographic printing and new electrodes produced by flexographic printing using commercially available inks, and investigated the scope to combine them with various electrolytes to construct a range of supercapacitors.

A supercapacitor needed high-surface-area electrode material, its resistance needed to be as low as possible to achieve high power and its energy storage was strongly affected by the electrolyte's electrochemical stability window.

Trials with the new electrodes in 6-molar potassium hydroxide with a filter paper separator had given realistic electrical results, but there were issues regarding sealing and electrode wetting.

A solid-state version had been developed, by coating each electrode in a PVA gel and allowing it to dry, then gluing the two electrodes

Rechargeable printed power sources



Dr Darren Southee

High-performance low-cost power modules



Professor Mark Johnson

together using the same gel and allowing the assembly to partially dry before sealing. No additional separator was required. A stack of supercapacitors charged to 2.4 volts had been shown capable of powering a 1.6 volt LED for around 90 seconds.

In a second demonstration, the printed electrodes were modified by adding an activated carbon layer and an ionic liquid was used as the electrolyte. The two electrodes were separated using filter paper and two supercapacitors were connected in series. In this combination, the supercapacitors could be charged to 6 volts, with a capacitance of around 0.5 Farad, and could light a wind-up torch for over a minute.

Professor Mark Johnson from the University of Nottingham

opened the afternoon session with a presentation on high-performance low-cost power modules for energy smart network applications.

He made it clear that power electronics was an essential part of the world's energy future, underpinning the whole low-carbon energy supply chain and controlling the conversion of electricity from one form to another and the energy flow which provided for grid quality and security.

Voltage source converters based on IGBT (insulated-gate bipolar transistor) switches were the building blocks for existing and emerging network applications, and in many cases it was necessary to interface converters directly to AC voltages in excess of 11kV (and up to 400kV). Individual semiconductor switches were rated to 6.5kV or less so either series connection of devices or series connection of converter cells was needed.

Professor Johnson described a voltage source converter of seriesconnected cells with "N+1" redundancy, so that the converter could continue to operate if any one cell failed, provided that it failed to a stable short circuit.

Most conventional IGBTs were supplied as plastic-packaged power modules. Assembly was time consuming and involved multiple solder processes and many ultrasonic bond wires, which tended to be potential weak points from the point of view of reliability: under extreme overload, each wire would act as a fuse and fail disruptively to an open circuit.

To satisfy the application requirements of high isolation voltage, minimised switching losses, excellent cooling performance, high reliability and a preference for fail-to-stable-short-circuit characteristics, together with a simplified assembly process, the research programme had been concentrated on electro-thermal design, bonding technologies, interconnect technologies and contact-interconnect technologies.

A planar power module had been designed with a compact volume and the ability to block high voltages, featuring failure-to-short-circuit behaviour with no bond-wires or bus bars.

After extensive evaluation and measurement, sintered silver nanoparticle pastes had been chosen as the best bonding method for achieving thermo-mechanical reliability of die attachment and interconnect, and a mechanically constrained flexible PCB gave the desired failure-to-short-circuit behaviour.

Assembly was a three-step process of silver sintering to attach silicon dies and bond flexible PCBs and metal bumps between two directbonded-copper substrates, followed by mounting of the sintered halfbridge onto the plastic frame and injecting silicone gel under vacuum to fill the gaps in the sub-assembly. Finally, a double side cooler was fitted.

Under static electrical test, the assembled modules showed typical current-voltage characteristics of IGBTs and in overcurrent conditions they failed to the desired short-circuit state.

Further work was ongoing to refine the assembly process.

Additive manufacturing process successfully applied to the low-volume production of ceramic packages for use in intelligent sensor systems for condition monitoring



Dr Robert Kay

30-300 GHz frequency range for communications and sensing applications - Hollow Waveguides



Professor Ian Roberson

Dr Robert Kay from **Loughborough University** described how an additive manufacturing process had been successfully applied to the low-volume manufacture of ceramic packages for use in intelligent sensor systems for condition monitoring.

He explained that many industrial sectors required bespoke packages for remote sensor networks operating in harsh environments, and that ceramic packages offered the advantages of high reliability, hermetic sealing and the ability to withstand high thermal and mechanical shock. But the traditional production of ceramic substrates required templatebased manufacturing processes that were only cost-effective in large batch sizes. Also, their geometry was limited to 21/2D. Additive manufacturing offered a route to overcoming these limitations.

Of the seven methods recognised by the ASTM F42 committee on additive manufacturing technologies, the one termed *"material extrusion - a material selectively dispensed through a nozzle or orifice"*, was chosen for investigation, with a simple timer circuit as the feasibility demonstrator.

A basic 3D printer was fitted with a piezo-electrically actuated microdispensing head and used to deposit an alumina-based paste through a 150 micron nozzle. The substrate was built up in several layers by a sequence of dam-and-fill operations, and then fired at 1600°C.

The conductor pattern was then deposited using a silver-based low-temperature co-fired ceramic paste designed for screen printing, through a 200 micron nozzle, and the substrate was re-fired at 865°C.

Assembly was completed by dispensing solder paste, pick-andplacing the components and reflowing to produce a working timer unit by all-digital operations - no templates having been used at any stage of the process.

This work demonstrated the potential for additive manufacture to revolutionise the production of ceramic-based packages by enabling mass customisation, iterative product development and quickturnaround, cost-effective low volume production.

Professor Ian Roberson from **Leeds University** highlighted the significance of the 30-300 GHz frequency range for communications and sensing applications, and the need to combine high Q-factor passive components with integrated circuits for microwave and millimetre-wave System-in-Package technology.

There was a significant performance gap between stripline or conventional coplanar waveguides and traditional hollow rectangular waveguides. Substrate-integrated waveguides tended to be very lossy if they were dielectric-filled, and there was an urgent need to establish ways of making hollow versions to satisfy anticipated 5G system requirements. Laser-prototyping in low-temperature co-fired ceramic materials avoided tooling costs but process challenges such as delamination, cracking and poor conductivity remained.

The first approach to the creation of a hollow waveguide was to fabricate a blank ceramic component by laser machining and plate it with electroless copper. Selective plating could be achieved by applying a photoresist, patterning it and leaving a trench in the substrate by excimer laser machining, activating the exposed substrate then removing the resist and plating the activated areas with electroless copper. Mask projection enabled patterns to be directly machined in the substrate, and techniques had been developed to plate interior surfaces of channel structures using flow-through methods.

A second approach had been to use standard low-temperature cofired ceramic process steps, by a progressive lamination technique. The project had achieved several significant world firsts, including the hollow substrate integrated waveguide concept and a millimetre-wave hollow substrate integrated waveguide slot-array antenna. The loss characteristics of hollow substrate integrated waveguides were comparable to those of traditional rectangular waveguides, and with further development they could become a serious alternative.

Work was continuing in a number of directions: 5G+ applications, higher frequencies, systems integration and microsystems.

Professor Karl Ryder from **University of Leicester** described the development and evaluation of a soldering flux based on a class of ionic liquids known as a deep eutectic solvents.

He explained that these ionic liquids were composed of organic cations and complexed anions, acting like low-temperature molten salts. They were environmentally benign, with good thermal stability and unusual solvent properties, and were particularly effective in dissolving metal oxides. They had found many specialist applications in metal finishing, and had more recently been observed to show great potential as fluxes for difficult-to-solder metals without the need for aggressive acid activators.

An area of current development was the formulation of solder pastes for electronics assembly. Pastes were based on a mixture of ionic-liquid flux with gelling agents and solder powder, and required different attributes depending on the application.

A metal content of 88.5 wt% was typical for stencil printing, or 83.5 wt% for dispensing. The paste needed to be resistant to slumping, and to be tacky enough to hold components in position after placement. Sufficient flux was required to stay active during reflow, to clean the metal surface, to promote the wetting of metal surfaces and the coalescence of the solder powder, and to maximise the wetting interaction between substrate and solder.

Production trials at the Manufacturing Technology Centre had given remarkably good results, even on heavily oxidised bare copper and heat-passivated electroless nickel. Cleaning was necessary after soldering, but very low ionic contamination results could be achieved by washing in cold water with no added cleaning agent.

The ability of ionic liquid fluxes to promote soldering to electroless nickel had led to the development of an alternative solderable finish for printed circuit boards, named HASLEN - hot air solder levelling on electroless nickel, where the nickel formed a barrier layer and prevented copper-tin intermetallic growth, improving long-term reliability.

Dr Alex Robinson from the Nanoscale Physics Research Laboratory at **University of Birmingham** gave an account of the evolution of chemically amplified photo-resists for next-generation lithography.

He explained that microelectronic devices were created by doping, etching or metallizing a semiconductor wafer to selectively change its electronic properties, and that lithography was used to image a resist, which then protected certain areas of the substrate whilst other areas were modified.

The lithographic exposure and development step accounted for up to 40% of the manufacturing time. As feature sizes on microelectronic devices continued to shrink, the capability of the lithographic process became limited by wavelength and diffraction effects.

Various workaround techniques had been used, including optical proximity correction, phase-shifting masks, off-axis illumination and immersion lithography, and 45 nanometre feature sizes could be resolved.

But the leading semiconductor manufacturers were working at the 20 nanometre level, and an alternative approach was required. Molecular resists, based on photopolymerisable C₆₀ Fullerenes, offered a

Soldering flux based on a class of ionic liquids



Professor Karl Ryder

Photo-resists chemically amplified - for next-generation lithography



Dr Alex Robinson

The Journal of the Institute of Circuit Technology Vol.8 No.1Sup March 2015

solution: they had very high etch resistance and were capable of 20 nanometre resolution, but their photosensitivity was low, and they had to be coated by vacuum sublimation. Their sensitivity could be enhanced by chemical amplification using photo-acid generators.

Dr Robinson described the development of a family of extreme-UV photoresists, and how their parameters had been characterised quantified to establish their commercial feasibility in preparation for spinning-out a company named Irrisistible Materials to commercialise University of Birmingham research in materials for semiconductor fabrication.

Curing to sensing using microwave energy



Professor Marc Desmulliez

The final presentation of the conference came from **Professor Marc Desmulliez**, Head of Sensors, Signals and Systems at **Heriot Watt University**.

He discussed the design, simulation and test of a novel microwave applicator used to cure paste materials in microelectronics packaging in a paper entitled: *"From curing to sensing using microwave energy: a journey across several manufacturing capability readiness levels."*

Motivation for the project had arisen out of a desire within the semiconductor manufacturing and packaging industry to gain a productivity improvement from equipment that could selectively bond chips on a board or wafer without damaging electronic circuits at board or wafer level.

The objective then was to develop an open-ended 'microwave oven' for in-situ curing and bonding in microelectronics processing applications.

Research had proceeded on several fronts, including the design of the open-ended oven, RF modelling, multiphysics modelling, system integration, and characterisation of cured materials. The outcome was a new generation oven with a built-in pyrometer which had been successfully demonstrated. The device had an alternative application as a sensor for on-line detection of water in food products, and had already enabled substantial cost savings.

Professor Desmulliez commented that multidisciplinary approaches required many different classes of expertise, and the research did not necessarily follow a linear pattern. Reflecting upon the original inspiration for this project, his advice was *"Be prepared to be bold and try crazy things - especially on a Friday afternoon!"*

leMRC Industrial Director **Professor Martin Goosey** closed the conference and thanked all present for their support in sharing the success and achievements of the centre's funded research projects over its 10-year journey.

Pete Starkey,

I-Connect007, February 201

I am grateful to Vince Scothern for allowing me to use his photographs



Professor Martin Goosey

EIPC Winter Conference Munich, February 2015. Day 1

by Peter Starkey F.Inst.C,T,

Ninety delegates, eleven countries represented and a thoughtprovoking two-day programme on themes of reliability in PCB fabrication and assembly, copper cleaning and advanced material solutions, advanced imaging and soldermask, and how to make PCBs smart and ready for Industry. Add the further attractions of a keynote by Walt Custer and the chance to visit a military aircraft assembly plant: the formula for another highly successful EIPC Conference, this time close to Munich Airport. Cold and crisp - clear skies and snow on the ground but not on the roads.

EIPC Chairman Alun Morgan's introduction held the audience spellbound as he embarked on an excursion into the world of augmented reality: "See the world around us, layered with information, data and visualisations, through the use of a device." With reference to head-up displays, initially in fighter aircraft and increasingly in motor cars, and augmented reality headsets like the newly announced Microsoft HoloLens, he attempted a practical demonstration of the sort of effects that could be experienced. In the event, "Peppa Pig's Magic Camera App" for his iPad, and a cardboard headset with his iPhone placed inside, were maybe not the best-chosen contrivances to give the most convincing exemplification. But his performance was highly entertaining anyway!

Having extended his warm thanks to the companies who had supported the conference with sponsorship, Morgan introduced **Walt Custer** as the keynote speaker, without whose **Business Outlook** no EIPC Conference would be complete.

Custer's inimitable blend of guick-fire information and sharp-witted perception gave some grounds for optimism. His analysis, based on leading indicators and sector-by-sector trends, by geography, by technology and by end market, was comprehensive and authoritative. In his summary of the global economic situation, he observed that the Eurozone and the UK had started 2015 on slightly firmer footings compared to 2014, with leading indicators rising slightly. Among the Eurozone nations, growth was signalled in Germany, Spain, the Netherlands and Ireland. France contracted slightly, the downturns in Greece and Austria accelerated and Italy stagnated. Eastern Europe fared well in comparison, led by the Czech Republic and Poland. Elsewhere, the downturn in Russia deepened, Turkey stagnated, Switzerland fell into contraction and Brazil made mild growth. In the USA, the outlook was for further modest growth, although the pace of expansion had slowed. In Asia, growth continued in Japanese manufacturing, there was broad stagnation in China and mild expansions in South Korea, Taiwan, India and Vietnam. Prices of key commodities oil and copper were down, the US dollar, Swiss Franc and Chinese RMB were strong and the Japanese Yen was weak. Global purchasing managers' indices showed positive for USA, Europe, South Korea, Taiwan and Japan, with only China showing negative. And of the world's top 25 PCB companies, only one was European and four American (three after the takeover of Viasystems by TTM). And based on 2013 figures, European production represented 4.5% of a global total of \$59.4 Billion.

The European PCB industry had an acceptable year in 2014, with no spectacular growth and no spectacular collapses. The few companies that had gone out of business were all sub-10 million euro turnover.



EIPC Chairman Alun Morgan

2015 Business Outlook



Walt Custer

Five countries: Austria, Switzerland, Germany, France and UK accounted for about 80% of total European production, and ended 2014 at a similar level as in 2013. There were some minor shifts, but no major changes. Supplies to certain end-markets offered some protection against Asian competition. Small volumes per part-number and protection of IP quite often required close proximity of fabricator to customer. All five countries mentioned supplied to industrial electronics industries. In addition, each country had identified further individual niches in which they continued to excel: Switzerland in the medical industry; Austria and Germany in the automotive sector, France and UK in defence and aerospace.

There had been some set-backs for each industry, for example cuts in defence budgets, unfavourable rates of exchange. Export sanctions against Russia or reduction in investments showed isolated consequences and might intensify in 2015. However, similar volumes to 2014 were expected. Continuing concentration of suppliers was a cause for concern, and the choice of raw materials used for the manufacturing of specialties might narrow down. Whether or not this would turn out to be a threat to certain projects remained to be seen.

In conclusion, 2014 was a year of modest single-digit growth globally for most electronic supply chain sectors. Capital equipment sales grew much more. Global political unrest remained a major concern. The Greek financial situation was a worry, oil prices had plummeted and commodities such as copper had deflated. Major currency exchange rate fluctuations would impact trade. The euro was currently weak against the US Dollar, Chinese RMB and Swiss Franc, but strong against the Japanese Yen. New high volume products were emerging and if projections for the Internet of Things were realised, quantities could be huge.

Leading indicators were useful for tracking growth regionally, and they had recently risen slightly for a number of European countries. The outlook for Europe was that Eurozone manufacturing showed signs of pulling out of the doldrums at the start of 2015, but the rate of expansion remained disappointingly meagre, vindicating the ECB's decision to take drastic action to revive the economy by quantitative easing, which was expected to boost the euro area economy via improved business and consumer confidence and the weakening of the euro. The currency's fall should benefit exporting manufacturers in particular over coming months. Lower oil prices would also help reduce manufacturers' costs, with reduced fuel costs also freeing up more consumer income to spend on goods.

Custer's closing comment: *"2015 is the year to focus on higher-growth end markets and take share from your competition!"*

The theme of the first technical session, moderated by Alun Morgan, was reliability in PCB fabrication - how to achieve it and how to make it measurable, and the first speaker was IPC Master Trainer **Dr-Ing**

Thomas Ahrens form Trainalytics in Germany. His topic was "Controlling the right parameters for PCB survival during assembly."

In his definition, a reliable assembly process was one that continuously conformed with requirements. His quality factors were man, machine, method, material, milieu and measurement. Process fitness was related to precision and repeatability, and the purpose of process control was to select and keep materials within specification, parameters within tolerance, equipment in function and documentation up-to-date. Process fitness also required periodic training and certification, the changelings of new knowledge and reviewing comprehension, maintained know-how and skills management.

Controlling the right parameters for PCB survival during assembly



Dr-Ing Thomas Ahrens

The Journal of the Institute of Circuit Technology Vol.8 No.1Sup March 2015

He defined solderability as the overall fitness of a component for industrial soldering, commenting that whereas electronics standards defined solderability as wettability, physics had a different view: wettability depended on solder surface metallurgy, working temperature and flux activity. Solder heat requirement increased with heat capacity and mass of the parts to be joined, and heat resistance limited the solder profile in terms of maximum allowable time and temperature, emphasising that design must be matched to solder method. He reviewed wetting tests, solderable surfaces, base material properties and methods of quality verification, then showed many examples of PCB defects, some of which were revealed by soldering, some of which were caused by soldering.

Dr-Ing Ahrens concluded by quoting the First law of Thermodynamics: *"In any process, the total energy of the universe remains the same"* and continued: *"Seen from the back, energy conservation means that nothing comes from nothing"*. He advocated the Flow-Down Principle – a deliberate and orderly plan of action – with the philosophy that quality must be built-in, with an equal quality level in every step of the process.

Bill Birch, President of PWB Interconnect Solutions in Canada, spoke with great authority about the measurement of performance degradation in printed wiring board interconnections and dielectric material, commenting in his opening statement *"The best thing ever to happen to my company was RoHS!"*

He observed that random PCB-related defects found during assembly level testing and early in the end use environment continued to plague the electronics industry, commenting that existing specifications, test methodologies and quality screening techniques were inadequate to eliminate defects, and that lead-free assembly has exasperated the situation. HDI designs introduced more structures and increased risk. He believed that capital investment and automation were needed to remain competitive and that European and North American PCB manufacturers should utilise engineering solutions to counteract limited capital. In-house screening with innovative testing protocols could dramatically reduce the risk of premature defects and improve the understanding of manufacturing capability.

Reflecting upon the origin of random defects, Birch believed that PCB's could be built to be inherently weak if inadequate process controls were available, material was selected incorrectly or the product design hierarchy of influence was not fully understood. Most defects were latent, not findable with electrical test, and existing quality control techniques were based on visual examination, with statistically invalid sample sizes. Assembly precipitated weak structure into a failure.

Assembly and rework were the only times that the PCB experienced temperatures above the glass transition temperature of the base material. A good board could be broken due to poor design, materials that were not suitable to the severity and number of assembly cycles and ultimately the applied strain exceeds the strength. All PCB's had a "potential life", and exposure to assembly and rework determined how much "residual life" would remain.

Against this background, Birch went on to demonstrate how good test vehicle design was an imperative for meaningful measurement of the impact of assembly and the prediction of the life of the product, and that the design must duplicate specific product features in order to measure material degradation. Microsections were not needed – the testing was all done electrically – although IPC microsection coupons were included to satisfy military requirements. He went on to describe his proprietary equipment for the detection of delamination by capacitance testing, and for the detection of electrical breakdown in via

Measurement of performance degradation in printed wiring board interconnections and dielectric material



Bill Birch

Assessment of the reliability of flexible circuits



Dr Hans-Peter Klein

Electrochemical failures in Automotive electronics



holes by interconnection stress resistance testing, and explained how the results were interpreted.

With reference to the physical properties of laminates, particularly the significance of the absolute glass transition temperature in acceleration studies, he showed how to select the right accelerationfactor parameters.

He concluded by stating that predicting the product life cycle was not difficult if specific rules were followed, emphasising that the establishment of performance criteria should be a partnership task between PCB fabricator, assembler and OEM. The real questions were *"How good is good enough?"* and *"Should we be testing for reliability or survivability?"*

A fabricator's perspective on the assessment of the reliability of flexible circuits came from Dr Hans-Peter Klein from Dyconex in Switzerland, with an approach based on objective evidence. Dyconex's area of specialisation was medical implants, where complexity was very high, volumes were very low and failure was not an option. In deciding what test procedure to use, it was necessary to determine what stresses would generate the acceleration factors and what would be the failure mechanism, bearing in mind that the stress method must be appropriate and not change the physics of failure. And it was important to understand what changes in materials and process parameters would require a review of the assessment procedure.

The focus of his investigation was microvia reliability under thermomechanical stress conditions, and the current induced interconnection stress test that Bill Birch had just described was used to simulate reallife exposure. The chosen temperature range was ambient to 210°C and three acceleration models: Basquin's model, Coffin-Mansion's model and Norris-Landzberg's model were used to calculate acceleration factors. The number of IST cycles was determined to reflect assembly, shipping and implanted life. As expected, stress during PCB assembly outweighed all other temperature exposures, and the worst-case Basquin's Model was used further on to determine sample sizes for ongoing reliability monitoring and lot-acceptance testing. It was calculated that, in order to establish a statistical base for microvia reliability of 99% probability with 95% confidence, 94 IST test cycles were required.

He described design for reliability as a continuous cycle with application requirements, acceleration modelling, material and process design, interconnection stress testing and reliability evidence as key elements.

Next came an OEM viewpoint on product reliability, in a presentation by **Saskia Mattern** from Robert Bosch in Germany about **electrochemical failures in automotive electronics**. There were three factors contributing to electrochemical failure: humidity, ionic contamination and electrical bias, and failure could be reversible in the case of creeping current as detected by surface insulation resistance measurements, or irreversible in the case of electrochemical migration and dendrite growth. In a context of miniaturisation, higher voltages and currents and humid surroundings, increasing efforts had to be made to ensure reliability.

Ms Mattern discussed the effects of test coupon geometry on surface insulation resistance results and time-to-failure from electrochemical migration, then reviewed actual results after reflow soldering.

High reflow temperature profiles had been observed to give increased surface insulation resistance and reduced propensity to

Saskia Mattern

Challenges faced in avionics products with reference to product applications on mission helicopters



Thomas Lauer

electrochemical migration, and hence improved PCB reliability as a consequence of de-activation of flux residues. Individual fluxes were found to have a specific temperature, to be exceeded to ensure complete deactivation. And it had been shown that high solder mask dams were beneficial in reducing dendrite growth.

A second OEM perspective, this time concerned with avionics, was presented by **Thomas Lauer** from the UIm factory of Airbus Defence and Space in Germany, which had the benefit of its own PCB shop. He discussed the **challenges faced in avionics products with reference to product applications on mission helicopters**, which were configured according to requirement: *"Lots of black boxes. What's inside them and why do they cost so much?"* and satellites: *"In-service repair is not possible!"*

He listed the environmental stresses typically experienced by avionic assemblies: low and high temperatures, pressure variations, vibration, acceleration and humidity. There were consecutive challenges of longterm availability of existing designs and technologies to avoid recertification, additive challenges like *"whisker mitigated"* conditions for pure tin surfaces, and extended acceptability criteria, which were usually specified at Class 3. Product reliability references were mostly based on tin-lead solder joints and PCA designs, and *"typical limits"* for voids and blow holes were not applicable.

He demonstrated various concepts used for increasing reliability, such as standards for voiding within component packages, stress mitigation per design by underfill and corner- or edge-bonding, ruggedisation by stand-off adaption or package transfer, conformal coating for environmental protection and whisker mitigation, vacuum vapour-phase soldering, re-balling of SAC BGA packages with tin-lead, and reflow based gold removal. There could also be design adaptations, for example in the substrate material, thickness and layer construction of the PCB, stiffeners and mechanical adjustment of the printed circuit assembly, as well as the optimisation of special interconnection processes, alloys or surfaces. *"Some of the reasons the black boxes cost so much....."*

The first conference day concluded with a privileged visit to the Airbus Defence and Space facility at Manching, and this is reported in *Vol.8.No.2*

Pete Starkey, I-Connect007. February 2015

EIPC Winter Conference Munich, February 2015. Day 2

by Peter Starkey F.Inst.C,T,



Professor Martin Goosey

PCB signal integrity and impedance design



Martyn Gaudion

Impact of Copper Topography on Signal Loss in High Frequency Applications



Wim Ongenae

Stimulated by the visit to Airbus Defence and Space, relaxed and refreshed by an excellent conference dinner in downtown Munich and a good night's sleep, delegates were bright-eyed and attentive for the second day of the EIPC Winter Conference. The programme comprised two sessions of technical presentations, one on copper cleaning and advanced material solutions, and the other on advanced imaging and solder mask, with a final panel session on how to make PCBs smart and ready for Industry 4.0.

Professor Martin Goosey moderated the first session, which opened with a presentation from **Martyn Gaudion**, CEO of **Polar Instruments** in the UK and expert on PCB signal integrity and impedance design.

He discussed how modelling and measurement could work together to ensure reliable prediction of multi-GigaHertz transmission-line performance, with particular reference to the effects of copper surface roughness.

After briefly reviewing the main resistive and dielectric contributors to insertion losses, he focused on the "skin effect" - the tendency of current to flow progressively closer to the surface of a copper conductor at high signal frequencies, to the extent that at 10GHz, the current was carried in a skin depth of less than 1 micron.

If theoretical loss calculations assumed a smooth conductor surface, they could give seriously inaccurate results in the case real conductors. Copper surfaces were deliberately treated during foil manufacture and multilayer PCB fabrication to enhance their adhesion to resin, and these bonding treatments generally resulted in surface roughening, to greater or lesser extent depending on the application.

The surface roughness made a significant contribution to insertion loss, and needed to be taken into account in the loss calculation. *"Remember - what you think you made may not be what you actually made!"* Gaudion illustrated this with microsections and explained how a technique known as the Hammerstad Method could be used to measure roughness and derive correction factors.

The results of three measurement methods for insertion loss, Vector Network Analysis (VNA), Short Pulse Propagation (SPP) and Single Ended TDR to Differential Insertion Loss (SET2DIL) had been compared and it had been concluded that, with good coupon design and accurate microsectioning, excellent correlation between modelled and actual values could be achieved.

Gaudion's presentation set the scene perfectly for the next presentation, from **Wim Ongenae**, Sales and Marketing Director at MEC Europe in Belgium, entitled "Impact of Copper Topography on Signal Loss in High Frequency Applications". Ongenae introduced a new chemical bonding pre-treatment for copper which offered an alternative to traditional surface-roughening processes. This process resulted in a chemical, rather than mechanical, bond to laminating resin, and maintained an effectively smooth conductor surface. The process sequence began with a non-etching acid cleaner followed by the deposition of copper-tin-nickel alloy coating only 50-100 nanometres thick. This was then treated with a silane anti-tarnish, present as a monomolecular layer. The silane had a similar function to the bonding treatment on glass fabric in that it acted as a chemical coupling agent, New universal sprayable processes for copper pretreatment and activation



Dr Peter Amann

Etchant - recyclable and environmentally friendly etchant pre-treatment for copper



Sefan Hotz

Thermal management of PCBs



Martin Cotton

forming a covalent bond between the metal surface and the laminating resin and giving high adhesion without roughening the surface.

Adhesion testing with a range of low-loss prepregs had shown excellent results, superior to those obtained with conventional roughening treatments even after multiple reflow, and as a consequence of the smooth surface the transmission loss at 50 GHz was equivalent to that of untreated material and about 10dB/M less than could be achieved with other bonding treatments.

Dr Peter Amann from **KIV PCB ProfiChem** in Germany described a family of new universal sprayable processes for copper pre-treatment and activation that could be used at various key stages of PCB manufacture to improve first-pass yield and reduce cost.

He gave details of a formulation based on iron-sulphuric, replenishable with hydrogen peroxide, for cleaning and micro-etching copper prior to dry film photoresist application, which gave a finer surface texture than sodium perslphate, and one based on peroxidesulphuric which was successful with liquid photoresist.

For cleaning and activating prior to multilayer bonding, he recommended a nitric-peroxide formulation, which gave very reliable bonding results.

Similar chemistry was recommended, but in a two-stage configuration, for copper preparation prior to solder mask application.

In each case he gave operating conditions and replenishment schedules. For small-volume manufacturers who could not justify a separate pre-treatment line for every operation, he suggested a versatile multi-purpose line, with a series of process options and alternative turnout stations.

Sefan Hotz from **Atotech** in Germany introduced a recyclable and environmentally friendly etchant for copper pre-treatment.

The chemistry was based on iron and was compatible with both stainless steel and titanium equipment. A closed-loop electrolytic regeneration system simultaneously re-oxidised the iron from ferrous to ferric and electrodeposited copper as saleable metal.

The process gave a low-profile grain-boundary micro-etch and the resulting surface gave excellent solder mask adhesion. And the closed-loop concept eliminated the need for feed-and-bleed replenishment so that no copper-rich waste water was generated.

Final testing was taking place, with a view to releasing the process for sale during the first half of 2015.

And now for something completely different, although it still involved copper! Martin Cotton, Director of OEM Technology for Ventec International Group, looked at thermal management of PCBs from a designer's point of view. Traditionally, component-level thermal issues had been addressed with external or internal heat-sinks. He specifically mentioned "coins" - slugs of copper embedded in recesses in the circuit board under the hot-spots of critical components. The design rules were many and complex, particularly with respect to dimensioning and tolerancing when multiple coins were required. Several alternative concepts had been explored, either as separate sub - assemblies of fabricated as part of the PCB, and using thermal via holes for heat conduction. But recent developments in insulated metal substrate (IMS) materials offered a more straightforward solution, and overcame many of the issues associated with localised heat sinks by spreading the thermal

load over a wider area. Many grades of IMS were available and Cotton stressed that, whatever the nominal thermal conductivity in W/mK, the significant parameter was the actual thermal impedance, which took into account dielectric thickness as well. "To reduce the thermal impedance by half. double the thermal conductivity or halve the thickness of the dielectric."

From thermal impedance, the dialogue reverted to the subject of electrical impedance, with a presentation from **Alexander Ippich** of **Isola Group** in Germany.

He reported the results of a designed experiment to observe the influence of copper foils on impedance, DC line resistance and insertion loss.

A test coupon had been designed with five different line widths and routed on two layers, three coupons per panel, and three panels were manufactured for each combination of four different copper foil types and two different oxide-replacement bonding treatments. Standard midloss laminate and prepreg were used, in an 8-layer stack-up with the 1oz copper foils under evaluation on the signal layers 3 and 6. The foils evaluated were: matte-side treated very low profile, shiny-side treated very low profile, matte-side treated ultra-low profile and matteside treated ultra-low profile with adhesion promoter. The bonding treatments were 'standard' oxide replacement and low-etch oxide replacement.

Insertion loss, impedance and DC line resistance were measured and the coupons were subjected to repeated reflow and solder shock testing.

Ippich described the electrical test methods and discussed the results in detail. There was a significant difference in insertion loss between matte side treated very low profile foil and reverse treated very low profile foil, and insertion loss could be significantly reduced by going from very low profile to ultra-low profile foils. The addition of adhesion promoter to the ultra-low profile foil has no negative effect at 5 GHz. The use of a low-etch oxide replacement instead of a standard oxide replacement was seen to be beneficial regarding insertion loss. This was true for standard copper foil and also for lower profile copper foils.

Thermal stress testing included 6 times repeated reflow at 230°C as received, solder float testing 3 x 10 seconds at 288°C after preconditioning for 4 hours at 150°C, solder float testing 6 x 10 seconds at 288°C after preconditioning for 4 hours at 150°C, followed by cross-sectioning to check for degradation. All samples survived solder float testing with no delamination observed. Likewise, reflow simulation testing at 230°C showed no irregularities and no delamination.

The session on advanced imaging and solder mask was moderated by **Oldrich Simek**, owner of **PragoBoard** in the Czech Republic, and his first presenter was **Uwe Altmann** from **Orbotech** in Belgium.

Well-known for his knowledgeable introductions to new developments in imaging technology, Altmann reviewed the development history of laser direct imaging from the late 1990s to the present day, as a background to his description of Orbotech's latest innovation, the multi-wave laser.

The market demand was for the capability to image any resist, with high throughput, whilst maintaining the best in image quality and registration. The limitation of previous systems was that diode-pumped solid-state lasers could only produce a single UV wavelength. Primary imaging resists and solder masks had photoinitiator systems with different spectral responses, so a single wavelength could not necessarily achieve optimum photospeed over a range of products. The new multi-wave laser integrated 375nm and 405nm sources into the same head, with the ability to control their relative intensities to match a

Impedance - Influence of copper foils on impedance, DC line resistance and insertion loss - a designed experiment to observe..



Alexander Ippich

Laser direct imaging the multi-wave laser.



Uwe Altmann

The Journal of the Institute of Circuit Technology Vol.8 No.1Sup

March 2015

particular photoinitiator. Altmann explained that these two UV wavelengths affected the polymerisation mechanism in different ways, one tending to work downwards from the top surface of the resist whilst the other was reflected from the copper surface and worked in the opposite direction, resulting in very uniform polymerisation with less energy consumed. And he demonstrated this with SEM photographs showing perfectly straight sidewalls on resist 100 microns thick.

Orbotech's latest direct imager could achieve 18 micron resolution at a throughput of 150 double-sided panels per hour.

Solder masks - Ink-jet printed .



Don Monn

Solder masks -Photoimageable - effect of thermal stress.



Sven Kramer

Next to speak was **Don Monn, Taiyo** America's European Sales Manager, with a presentation on solder mask developments in the digital age. "*Before I tell you what I'm going to tell you, I'm going to tell you what I'm not going to tell you!*"

Speaking from his many years' practical experience of applying and imaging solder mask, he began by listing the limitations of the original technique, screen printing, then ticking them off one-by-one as technology advanced. His list included: registration issues, artwork, bleed, skips, exposed copper and uneven mask deposit.

Liquid photoimageable resolved some of the issues, but imaging still depended on artwork, and coating skips were still possible. Laser direct imaging resolved the artwork issue, but some coating issues remained although coating techniques had progressively improved.

"What's next?" he asked, keeping his audience in suspense whilst he tempted them with another list: "It won't require artwork, it won't require most typical processing equipment, it will create lots of space on the shop floor, and it will eliminate the three biggest challenges in the solder mask operation: registration, mask in holes and lost or missing dams." With a theatrical flourish, he unveiled a video showing solder mask being ink-jet printed. Although other suppliers' prior attempts at solder mask ink-jetting had been unsuccessful, Monn was confident that Taiyo, in cooperation with several manufacturers of ink-jet printing equipment, had formulated a product that would be rapidly adopted by the PCB industry.

Returning to the topic of photoimageable solder masks, **Sven Kramer** from **Lackwerke Peters** in Germany gave an overview of today's material capabilities and limitations, with a particular focus on their ability to withstand thermal stress. *"The first law of material science: Everything can be destroyed by force!"*

The most obvious effect of thermal stress on a solder mask was discolouration. What was an acceptable level, particularly for ultra-white materials used in LED applications? Was the ultimate degree of initial whiteness more important than the thermal stability of whiteness over time? He explored the failure mechanisms of solder mask under heatageing and thermal cycling conditions. The ageing process could result in loss of volatiles, oxidation, continuation of polymerisation, chemical separation of low-molecular-weight components or hydrolysis of polymers in the presence of moisture.

The effect of copper surface preparation on the thermal ageing of solder mask had been extensively studied by Peters, particularly in respect of adhesion, and chemical methods had been shown to give more consistent long-term adhesion than pumice scrubbing or mechanical brushing.

Long-term ageing testing had demonstrated that specialised liquid photoimageable solder masks now commercially available were capable of operating at 175°C, with adhesion and insulation performance at a similar level to standard coatings rated for 150°C long term resistance. Substrate pre-treatment had become increasingly important to

Independent Laboratory Recognition for Solder Resists



Emma Hudson

Industry 4.0 and Smart Manufacturing



Alexander Schmoldt

achieve the desired results, and it was necessary to use high-Tg substrates to avoid cracking resulting from thermal mismatches. It was not yet possible to offer products with long term 200°C thermal resistance. Although good adhesion to substrate could be maintained, insulation properties were degraded after long term exposure to 200°C, and the mechanism was not yet fully understood.

All this talk about solder resists - what about the formalities of gaining UL recognition for a solder resist and adding it to your UL-recognised PCB? With clear and straightforward explanations, **Emma Hudson,** Lead PCB Engineer at **Underwriters Laboratories**, guided the way through the UL system, pointing out whether additional testing would be necessary within the Solder Resist Recognition Programme, designed to make it easier for the PCB manufacturer to add new resists to their UL-recognized boards.

Ms Hudson made it clear that the primary concern with solder resists was the flammability hazard – did they add fuel to a fire? UL recognition showed a commitment to safety and provided the customer with added reassurance that an independent party had tested and would continue to verify the material on a regular basis.

Provided certain conditions were satisfied, the Permanent Coating Program in UL 796 allowed PCB manufacturers to add recognised resists to existing board types without any additional testing. And UL recognised solder resists could be cheaper and quicker for a PCB manufacturer to start using than unrecognised materials She explained the requirements for gaining recognition of a solder resist, the requirements for improving recognition of an existing solder resist, considerations when adding a new solder resist to an existing rigid PCB and whether additional testing was required. With the re-classification of FR4 laminates, re-testing would be required if moving from FR4.0 to FR4.1.

More resists were being recognised in multiple colours, but it was not mandatory to test every colour to gain all-colour recognition, only the "worst-case" examples: no-colour, black, white and red. Reduced test programmes could be used to extend recognition of an existing resist to additional UL/ANSI grades or to improve other parameters. Ms Hudson suggested that solder resist suppliers and PCB manufacturers should consider partnering when proposing to add a resist to a different UL/ANSI grade.

The final session of the conference was an open discussion on Industry 4.0 and Smart Manufacturing, led by "*a panel of industry experts*" and moderated by **Alexander Schmoldt** from **Murata** in Germany, who explained that Industry 4.0 - effectively the fourth industrial revolution - was about the technical incorporation of cyber physical systems in production and value chain logistics, and the integration of the Internet of Things concept into industrial processes. It would have important consequences in value creation and business models and would significantly affect the organisation of the work force. A basic paradigm change would be required: production in the "Smart Factory": through "Smart Automation" interacting with "Smart Products", each with a digital ID to enable new cloud-based services and business models.

Schmoldt considered the example of a Smart Factory manufacturing electronics, where an obvious way to make products "Smart" was to add an RFID function to their printed circuit boards, so that they each had a unique communication address and memory. The panel discussed the options for adding RFID to PCBs, by embedding an RFID

into the board, or by adding an RFID module as a component during the assembly process. Various types of RFID devices were compared, and actual case studies were used to illustrate how the added value of smart PCBs benefited different stakeholders over the product life cycle. Panel members Stephan Kunz from Schmoll Maschinen, Norbert Heilmann from ASM Assembly Systems and Torsten Bethke from Micronex each gave short presentations: Stephan Kunz demonstrated automated equipment for the embedding of UHF RFID chips in the edge of circuit boards, which was already being used commercially. Norbert Heilmann discussed the benefits and limitations of PCBs with embedded RFID in the assembly process, from the viewpoint of a manufacturer of assembly equipment. Torsten Bethke gave the views of an EMS provider, who saw serious challenges to human resources and the inevitability of a demographic change, where unskilled workers would be the losers. And there was concern from some members of the audience that the Internet of Things could lead to too much information being available to too many people and organisations, and that personal privacy was increasingly under threat.









Stephan Kunz

Norbert Heilmann

Torsten Bethke

In his closing summary, Schmoldt concluded that Industry 4.0 inevitably required smart products, and that RFID was recognized as a standard means to create smart objects. RFID in electronics 4.0 means source tagging of electronic products and RFID embedded into the PCB is the ideal means for a cradle to cradle approach, making cyclical and sustainable business models possible. The deployment of RFID infrastructure in electronics production had just begun, and presented business opportunities for systems integrators, hardware and software manufacturers. Many successful user-examples already existed in the industry, and had demonstrated the benefits of RFID to SMEs as well as large OEMs.

Alun Morgan brought proceedings to a close, once again acknowledging the support of the sponsors and thanking the presenters for sharing their knowledge, the delegates for their attention and, in particular EIPC Executive Director **Kirsten Smit-Westernberg** and Event Manager **Sonia Derhaag** for their faultless organisation and coordination of another hugely successful conference.

Pete Starkey,

I-Connect007, February 2015

I am grateful to Alun Morgan for allowing me to use his photographs.

Corporate Members of The Institute of Circuit Technology March 2015

Organisation	Address	Communication	
Adeon Technologies BV	Weidehek 26, 4824 AS Breda, The Neth	+31 (0) 76-5425059 <u>www.adeon.nl</u>	
ALR Services Ltd.	Unit 9 Thame Business Park , Thame, Oxc	on OX9 3XA	01844 217 487 www.alrpcbs.co.uk
Anglia Circuits Ltd.	Burrel Road, St.Ives, Huntingdon	PE27 3LB	01480 467 770 www.angliacircuits.com
Atotech UK Ltd.	William Street, West Bromwich.	B70 OBE	0121 606 7777 www.atotech.com
CCE Europe	Wharton Ind. Est., Nat Lane, Winsford	CW7 3BS	01606 861 155 www.ccee.co.uk
ECS Circuits Ltd.	Unit B7, Centrepoint Business Park, Oak I Dublin 12, Ireland	Road,	+353-(0)1-456 4855 _www.ecscircuits.com_
Electra Polymers Ltd.	Roughway Mill, Dunks Green, Tonbridge	TN11 9SG	01732 811 118 www.electrapolymers.com
The Eurotech Group	Salterton Industrial Estate, Salterton Road Exmouth	EX8 4RZ	01395 280 100 www.eurotech-group.co.uk
Falcon Group	Riverside Ind. Est. ,Littlehampton	BN17 5DF	01903 725 365 www.falconpcbgroup.com
Faraday Printed Circuits Ltd	15-19 Faraday Close, Pattinson North Ir Washington.	nd. Est., NE38 8QJ	01914 153 350 www.faraday-circuits.co.uk
Graphic plc	Down End, Lords Meadow Ind. Est., Crediton	EX17 1HN	01363 774 874 www.graphic.plc.uk
GSPK (TCL Group)	Knaresborough Technology Park, Manse L Knaresborough	ane HG5 8LF	01423 798 740 www.gspkcircuits.ltd.uk
Invotec Group Ltd	Hedging Lane, Dosthill , Tamworth	B77 5HH	01827 263 000 www.invotecgroup.com
PMD (UK) Ltd.	Broad Lane, Coventry	CV5 7AY	02476 466 691 <u>sales@pmdgroup.co.uk</u>
Rainbow Technology Systems	40 Kelvin Avenue, Hillington Park Glasgow	G52 4LT	01418 923 320 www.rainbow-technology.com
Spirit Circuits	22-24 Aston Road, Waterlooville, Hampshire	PO7 7XJ	02392 243 000 info@spiritcircuits.com
Stevenage Circuits Ltd	Caxton Way, Stevenage.	SG1 2DF	01438 751 800 www.stevenagecircuits.co.uk
Ventec Europe	1 Trojan Business Centre, Tachbrook Park Leamington Spa	01926 889 822 www.ventec-europe.com	
Zot Engineering Ltd	Inveresk Industrial Park Musselburgh, B19 I) EH21 7UQ	0131-653-6834 www.data@zot.co.uk