Calculating Specifying and Testing Electrical Characteristics of PCB’s

Neil Chamberlain
European Sales Manager
www.polarinstruments.com
Speedstack PCB
Automatic impedance controlled
PCB stackup design & documentation

Polar Instruments
Agenda

• Why Controlled Impedance
• Calculating Impedance
  – Modelling
  – FR4 Issues
• Specify Impedance
  – Correct Calculations
  – Correct Documentation
• Testing Impedance
  – Coupon Design
  – TDR Testing
  – Testing for Loss

© Polar Instruments 2009
www.polarinstruments.com
Why Impedance Matching

• Controlling Signal Noise
• Signal Termination
  – Xaui
  – Rocket I/O
• Specification
  – USB 2
  – PCi Express
  – DDR 3
• RF Filtering
Accurate Impedance Calculation

• Simulate Trace Geometries
• Use Accurate Model

• Requires a 2d Field solver
Trapezoidal Model

- Two input parameters required for Trace Width
- Models the Print and Etch process within the PCB Manufacture

These numbers can be provided by your PCB Manufacture
Solder Mask Modelling

- Solder mask has a large effect on impedance on surface traces
- Depending on Geometry can be as large as 5Ω
Resign Modeling

- Both are Mixtures of Resin and Glass Fibers
  - Materials are non-homogenous
    - $\varepsilon_r$ specified for laminate is the bulk value
    - $\varepsilon_r$ for glass $\sim 6.1$ $\varepsilon_r$ for epoxy $\sim 3.2$
  - So significant local variations occur for $\varepsilon_r$
Typical E-field distribution

Embedded Microstrip

© Polar Instruments 2009
www.polarinstruments.com
Microphotograph of FR4 structure

Core

Glass fibers $Er = 6$

Resin $Er = 3.2$

Prepreg

C

P

C

5 mil
FR4 structure

- $Er = 6.0$
- $Er = 3.2$
- Bulk $Er$ value in this direction is 4.2 approx
Field in FR4 structure
Field distribution in Differential Pair

Impedance value
Increases as
Er and C decrease
All Models are Wrong

But Some are Useful !!

Tolerance needs to be given on all Simulated results
Modelling Losses

• Designers need to concern themselves with Loss as well as Impedance
• Frequency Dependant Modelling
• Low Dk Material Modelling
Modelling Loss
Modelling Loss
So How do we get the modelled results to the fabricator

Document your stacks like this:
And like this:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Stack-up</th>
<th>Supplier</th>
<th>Supplier Description</th>
<th>Impedance ID</th>
<th>Description</th>
<th>Processed Thickness</th>
<th>Sr</th>
<th>Data Filename</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Polar Samples PE/001</td>
<td>Flexible Mask</td>
<td>PE001</td>
<td>Primary-Side-PEable-P1.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Polar Samples ID/001</td>
<td>Screened Ident</td>
<td>ID001</td>
<td>Primary-Side-Ident-L1.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>Polar Samples SM/001</td>
<td>Liquid Photographic Mask</td>
<td>SM001</td>
<td>Primary-Side-Solder-Mask-1.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Polar Samples FO/001</td>
<td>Copper Foil</td>
<td>FO001</td>
<td>Primary-Side-L1.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>Polar Samples PP/001</td>
<td>PrePreg 1680</td>
<td>PP001</td>
<td>Ground-Plane/Inner-Tracking-L2.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>Polar Samples CO/020</td>
<td>FR4 Core</td>
<td>CO020</td>
<td>Inner-Tracking-L3.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>Polar Samples PP/003</td>
<td>PrePreg 3113</td>
<td>PP003</td>
<td>Inner-Tracking-L3.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Polar Samples PP/003</td>
<td>PrePreg 3113</td>
<td>PP003</td>
<td>Inner-Tracking-L3.ger</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- Copper Thickness = 11.200
- Dielectric Thickness = 21.340
- Overall Processed Thickness = 20.540

<table>
<thead>
<tr>
<th>Impedance ID</th>
<th>Structure Name</th>
<th>Impedance Signal Layer</th>
<th>Reference Plane 1 in Layer</th>
<th>Reference Plane 2 in Layer</th>
<th>Trace Separation</th>
<th>Ground Plane Separation</th>
<th>Lower Ground Plane Width</th>
<th>Lower Ground Strip Width</th>
<th>Calculated Impedance</th>
<th>Target Impedance</th>
<th>TOL (± %)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Coated Microstrip 1B</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>4.25</td>
<td>0.09</td>
<td>0.00</td>
<td>0.00</td>
<td>49.38</td>
<td>50.00</td>
<td>10.00</td>
</tr>
<tr>
<td>2</td>
<td>Offset Coplanar Stipes 1B/A</td>
<td>3</td>
<td>2</td>
<td>4</td>
<td>19.00</td>
<td>0.09</td>
<td>8.00</td>
<td>19.00</td>
<td>27.84</td>
<td>28.00</td>
<td>10.00</td>
</tr>
<tr>
<td>3</td>
<td>DRI Embedded Coplanar Waveguide With Lower Ground 1B/A</td>
<td>7</td>
<td>5</td>
<td>0</td>
<td>12.00</td>
<td>8.09</td>
<td>27.00</td>
<td>6.00</td>
<td>100.51</td>
<td>100.00</td>
<td>10.00</td>
</tr>
<tr>
<td>4</td>
<td>Coated Microstrip 1B</td>
<td>6</td>
<td>5</td>
<td>0</td>
<td>20.00</td>
<td>0.09</td>
<td>75.00</td>
<td>7.00</td>
<td>75.00</td>
<td>75.00</td>
<td>10.00</td>
</tr>
</tbody>
</table>

© Polar Instruments 2009
www.polarinstruments.com
Even Document Flex Rigid Like this:
Why is stackup design and communication important?

• Time to market
• Complex designs
• Communication from designer to PCB fabricator
• Increasing impedance requirements
• Can be time consuming
• Good communication saves costly rebuilds
Material Libraries

• Based on the parameters of actual material.

• Separated into material types
  – Cores
  – Prepregs
  – Foils, etc.
The info required for cores

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Supplier Description</th>
<th>Description</th>
<th>Stack Number</th>
<th>Dielectric Base Thickness</th>
<th>Dielectric Finished Thickness</th>
<th>Dielectric Constant</th>
<th>Upper Cu Base Thickness</th>
<th>Lower Cu Base Thickness</th>
<th>Resin Content</th>
<th>Tg</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>ISO443</td>
<td>2-2165</td>
<td>06404NTS</td>
<td>0.254</td>
<td>0.254</td>
<td>4.71</td>
<td>0.016</td>
<td>0.018</td>
<td>47.4</td>
<td>140</td>
<td></td>
</tr>
</tbody>
</table>

© Polar Instruments 2009
www.polarinstruments.com
Will it fit?!!

Keep track of board thickness.
Check that it meets design rules
Adding a controlled impedance structure

Add a structure on your selected layer
Finished thickness calculation:

Calculate finished thickness (choice of methods).
Document conventional laser blind buried and stacked vias.
Coupon Testing
TDR Testing

• Testing is not difficult or Time consuming
• Required for Process conformance to Specification.
• MVT not DVT.
The Future of testing:- Atlas

- New high speed busses in Multi GHz range
  - SuperSpeed USB 3.0
  - PCI Express Gen 2.0
- Differential Signalling techniques allow the continued uses of FR4
- Requires accurate control of transmission line losses
The Future of testing: - Atlas
Atlas Coupon Test
Conclusion

• Accurate Modelling is as important as final testing.
• Material selection is critical to the performance of the final product
• Clear Documentation is imperative
• Testing final product is made easy through robust test system.
Thank You

• Questions?....

Neil@polarinstruments.com

www.polarinstruments.com